

Analog Peripherals

10-Bit ADC

- ± 1 LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor (± 3 °C)

Two 12-Bit DACs

- Voltage output
- 10 μ sec settling time

Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

Internal Voltage Reference

V_{DD} Monitor/Brown-out Detector

On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

High-Speed 8051 μ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

Memory

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

Clock Sources

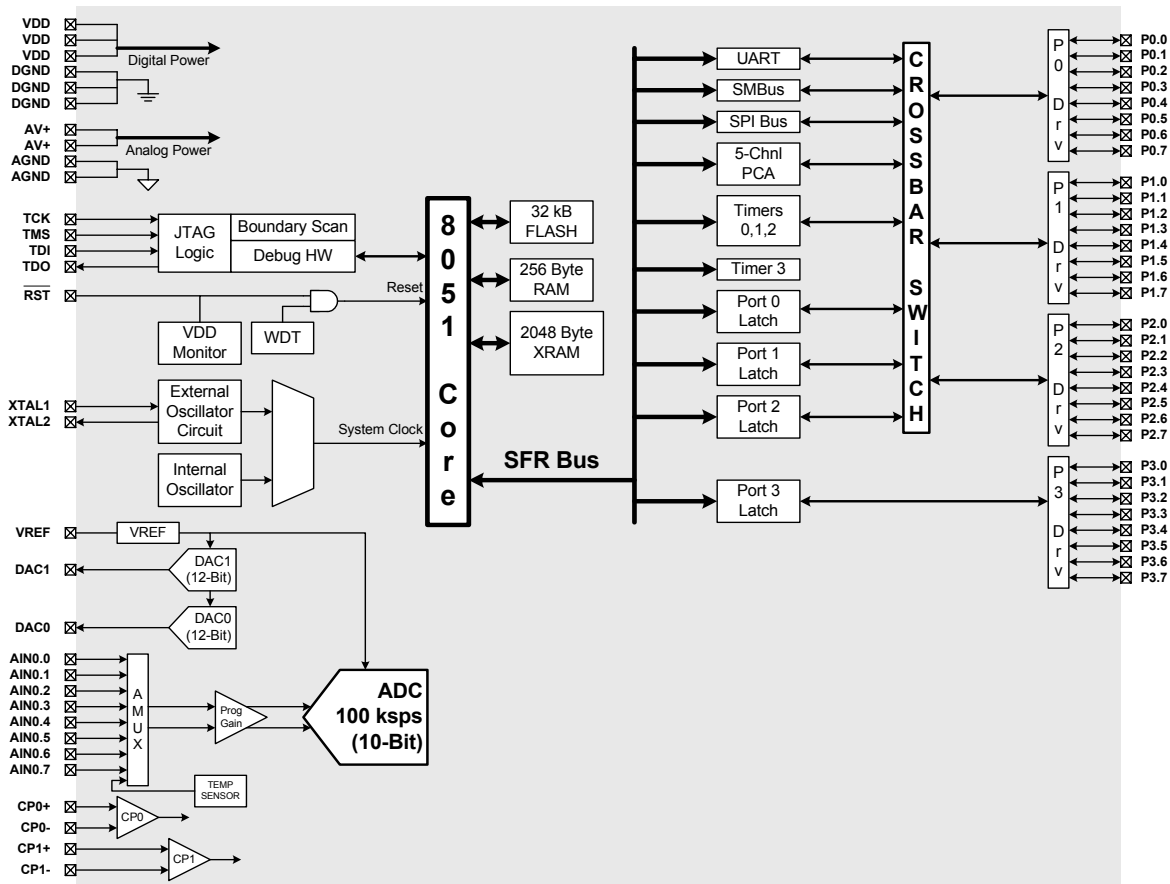
- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

Supply Voltage: 2.7 to 3.6 V

- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

64-Pin TQFP

Temperature Range: -40 to $+85$ °C

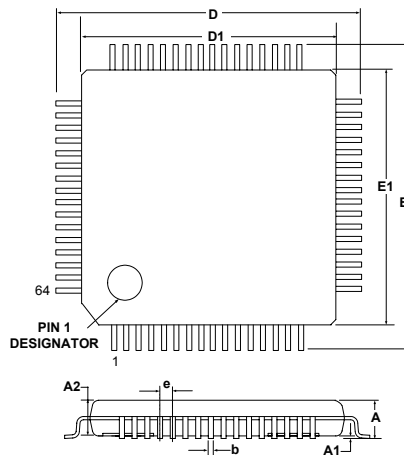


Selected Electrical Specifications

($T_A = -40$ to $+85$ C°, $V_{DD} = 2.7$ V unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL CHARACTERISTICS					
Analog Supply Voltage		2.7		3.6	V
Analog Supply Current	Internal REF, ADC, DAC, Comparators all active		0.8		mA
Analog Supply Current with analog sub-systems inactive	Internal REF, ADC, DAC, Comparators all disabled		5		μA
Digital Supply Voltage		2.7		3.6	V
Digital Supply Current with CPU active	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz		12 0.5 20		mA mA μA
Digital Supply Current (shutdown mode)	Oscillator not running		2		μA
V_{DD} Data Retention Voltage	RAM remains valid		1.5		V
CPU & DIGITAL I/O					
Clock Frequency Range		DC		25	MHz
Port Output High Voltage	$I_{OH} = -3$ mA, Port I/O push-pull	$V_{DD} - 0.7$			V
Port Output Low Voltage	$I_{OL} = 8.5$ mA			0.6	V
Input High Voltage		$0.8 \times V_{DD}$			V
Input Low Voltage				$0.2 \times V_{DD}$	V
SMBus SCL Frequency	SYSCLK = MCU system clock			SYSCLK/8	MHz
SPI Bus Clock Frequency	SYSCLK = MCU system clock			SYSCLK/2	MHz
A/D CONVERTER					
Resolution		10			bits
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
Throughput Rate				100	ksps
Input Voltage Range		0		V_{REF}	V
D/A CONVERTERS					
Resolution		12			bits
Integral Nonlinearity	Specified from Data Word 014h to FEBh		±4		LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
Offset Error	Data Word = 014h		±3		LSB
Output Settling Time	To ½ LSB of full-scale		10		μs
Output Voltage Swing		0		$V_{REF} - 1$ LSB	V
COMPARATORS					
Supply Current	(each Comparator)		1.5		μA
Response Time	$ (CP+) - (CP-) = 100$ mV		4		μs
Input Voltage Range		-0.25		(AV+) +0.25	V
Input Bias Current		-5	0.001	+5	nA
Input Offset Voltage		-10		+10	mV

Package Information



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	-	1.05
b	0.17	0.22	0.27
D	-	12.00	-
D1	-	10.00	-
e	-	0.50	-
E	-	12.00	-
E1	-	10.00	-

C8051F005DK Development Kit

