

### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Supply Voltage: 2.7 to 3.6 V

- Typical operating current: 6.4 mA at 25 MHz  
9  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 4 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

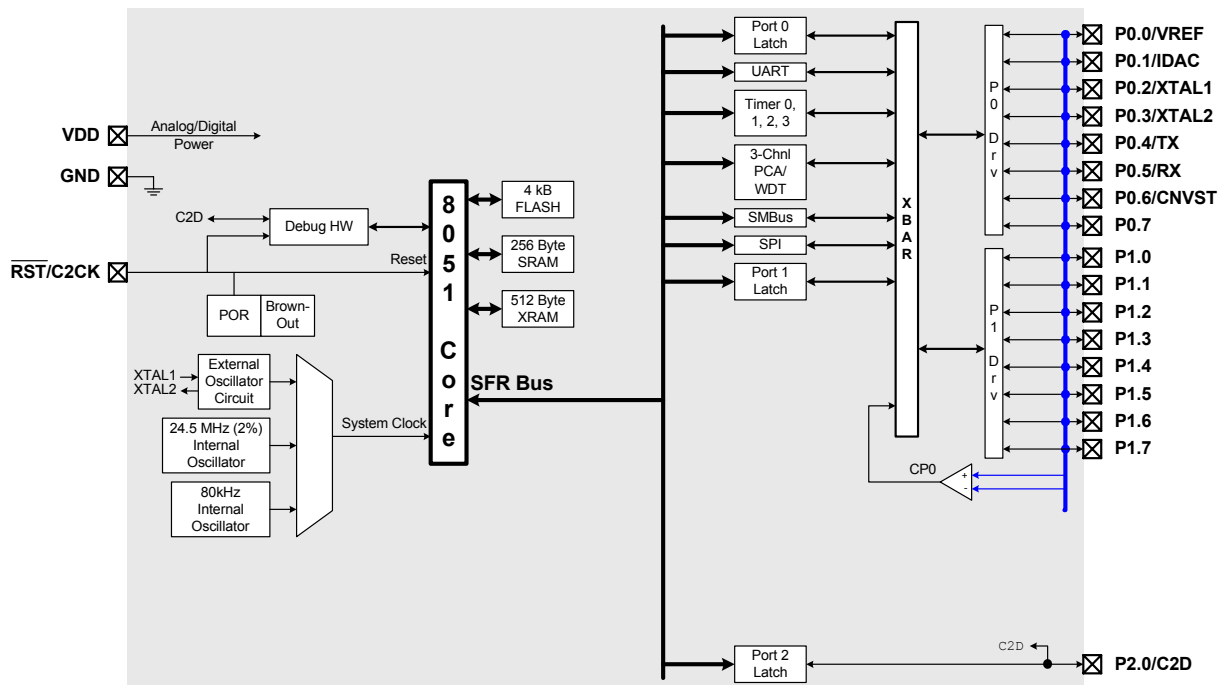
- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Package

- 20-Pin QFN (lead-free package)

### Ordering Part Numbers

- C8051F333-GM

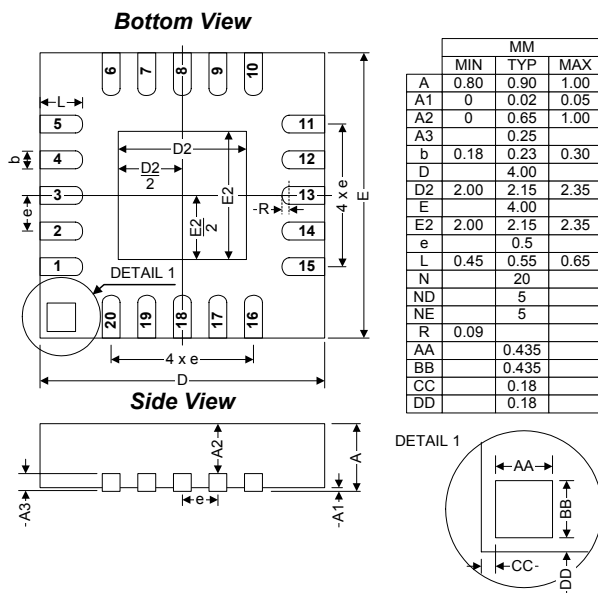


### Selected Electrical Specifications

( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  V unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
<b>Global Characteristics</b>					
Supply Voltage		2.7		3.6	V
Supply Current with CPU active	Clock = 25 MHz	—	6.4	—	mA
	Clock = 1 MHz	—	0.36	—	mA
	Clock = 80 kHz; $V_{DD}$ Monitor Disabled	—	20	—	$\mu$ A
Supply Current (shutdown)	Oscillator off; $V_{DD}$ Monitor Disabled	—	<0.1	—	$\mu$ A
Clock Frequency Range		DC	—	25	MHz
<b>Internal Oscillators</b>					
Frequency (OSC0)		24.0	24.5	25.0	MHz
Frequency (OSC1)	See Note	—	80	—	kHz
<b>Comparator</b>					
Response Time Mode0	(CP+) – (CP-) = 100 mV	—	0.1	—	$\mu$ s
Current Consumption Mode0		—	7.6	—	$\mu$ A
Response Time Mode1	(CP+) – (CP-) = 100 mV	—	0.18	—	$\mu$ s
Current Consumption Mode1		—	3.2	—	$\mu$ A
Response Time Mode2	(CP+) – (CP-) = 100 mV	—	0.32	—	$\mu$ s
Current Consumption Mode2		—	1.3	—	$\mu$ A
Response Time Mode3	(CP+) – (CP-) = 100 mV	—	1	—	$\mu$ s
Current Consumption Mode3		—	0.4	—	$\mu$ A
<b>Note:</b> OSC1 can be calibrated in 2.5% steps using an internal calibration register.					

### Package Information



### C8051F330DK Development Kit

