Si4113G-X5

RF Synthesizer With Integrated VCOs For Dual and Triple-Band GSM and GPRS Wireless Communications

Features

- RF synthesizers
  - RF1: 1400 MHz to 1.8 GHz
  - RF2: 1200 MHz to 1.5 GHz
- Integrated VCOs, loop filters, varactors, and resonators
- Minimal (2) external components required
- Infineon SMARTi and SMARTi+ compatible
- GPRS Class 12 compliant
- Settling time: 140 μs
- Low phase noise
- Programmable powerdown modes
- 1 μA standby current
- 2.7 V to 3.6 V operation
- Package: 28-lead, 5 x 5 mm MLF package (MLP)

Ordering Information:

See page 22.

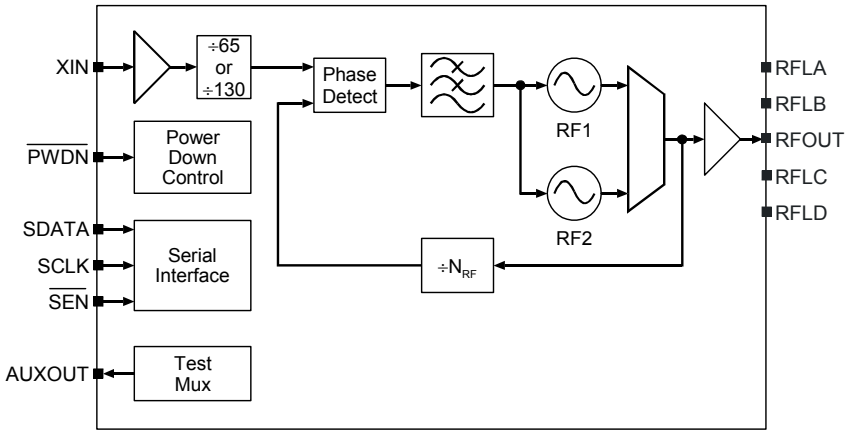
Applications

- E-GSM 900, DCS 1800, and PCS 1900 mobile handsets
- GPRS handsets and data terminals
- HSCSD data terminals

Description

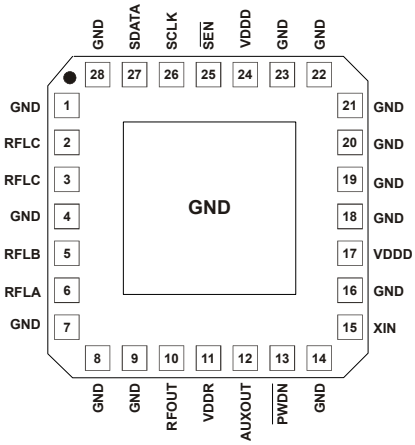
The Si4113G-X5 is a monolithic integrated circuit that performs RF synthesis for dual and triple-band GSM and GPRS wireless communications applications. The Si4113G-X5 includes two VCOs, loop filters, reference and VCO dividers, and phase detectors. Divider and powerdown settings are programmable through a three-wire serial interface.

Functional Block Diagram



Pin Assignments

Si4113GX5-BM



Patents pending

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Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–20	25	85	°C
Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Supply Voltages Difference	V_Δ	($V_{DDR} – V_{DDD}$), ($V_{DDI} – V_{DDD}$)	–0.3	—	0.3	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at 3.0 V and an operating temperature of 25°C unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 4.0	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	–55 to 150	°C

Notes:

1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **This device is a high performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.**
3. For signals SCLK, SDATA, $\overline{SEN}$, $\overline{PWDN}$ and XIN.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF1 Mode Supply Current[1]		RF1 active	—	13	17	mA
RF2 Mode Supply Current[1]		RF2 active	—	12	17	mA
Standby Current		$\overline{PWDN}$ = 0	—	1	—	µA
High Level Input Voltage[2]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[2]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[2]	I_{IH}	V_{IH} = 3.6 V, V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IL} = 0 V, V_{DD}= 3.6 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OH} = 500 µA	—	—	0.4	V

Notes:
1. RF1 = 1.54 GHz, RF2 = 1.36 GHz
2. For signals SCLK, SDATA, $\overline{SEN}$, and $\overline{PWDN}$.
3. For signal AUXOUT.

Table 4. Serial Interface Timing
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{clk}	Figure 1	40	—	—	ns
SCLK Rise Time	t_r	Figure 1	—	—	50	ns
SCLK Fall Time	t_f	Figure 1	—	—	50	ns
SCLK High Time	t_h	Figure 1	10	—	—	ns
SCLK Low Time	t_l	Figure 1	10	—	—	ns
SDATA Setup Time to SCLK↑[2]	t_{su}	Figure 2	5	—	—	ns
SDATA Hold Time from SCLK↑[2]	t_{hold}	Figure 2	0	—	—	ns
$\overline{SEN}$↓ to SCLK↑ Delay Time[2]	t_{en1}	Figure 2	10	—	—	ns
SCLK↑ to $\overline{SEN}$↑ Delay Time[2]	t_{en2}	Figure 2	12	—	—	ns
$\overline{SEN}$↑ to SCLK↑ Delay Time[2]	t_{en3}	Figure 2	12	—	—	ns
$\overline{SEN}$ Pulse Width	t_w	Figure 2	10	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform, unless otherwise noted.
2. Timing is not referenced to 50% level of waveform. See Figure 2.

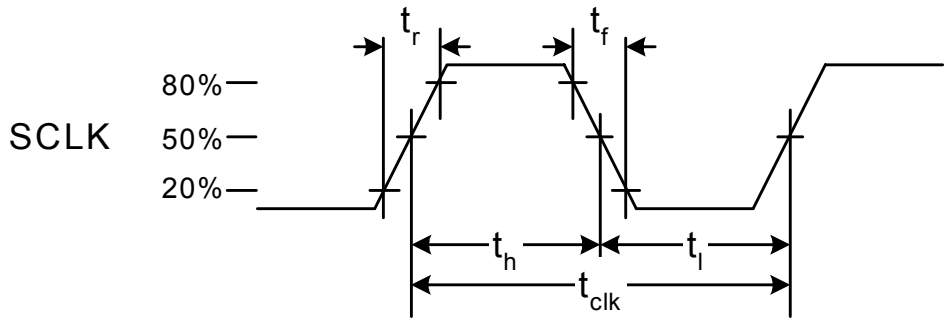


Figure 1. SCLK Timing Diagram

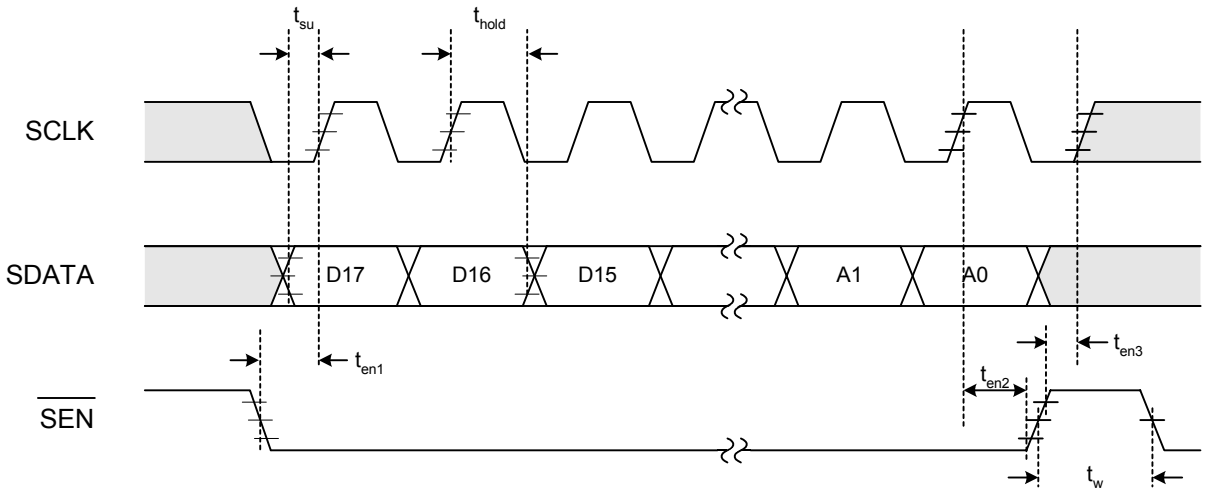


Figure 2. Serial Interface Timing Diagram

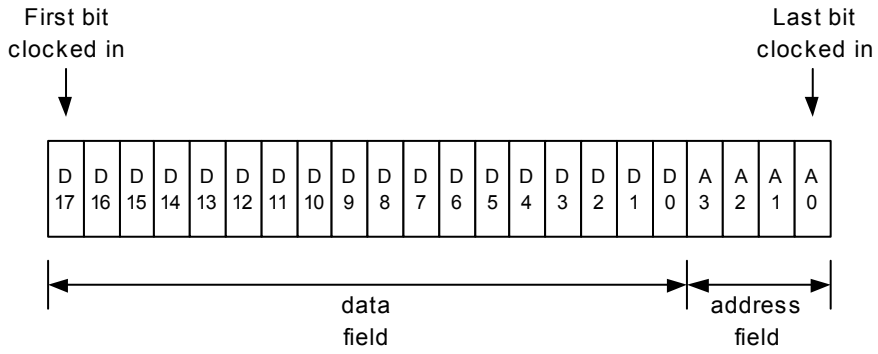


Figure 3. Serial Word Format

Table 5. RF Synthesizer Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
XIN Input Frequency	f_{REF}		13	—	26	MHz
Reference Amplifier Sensitivity	V_{REF}		0.5	—	V_{DD} +0.3	V_{PP}
Phase Detector Update Frequency	f_ϕ	$f_\phi = f_{REF}/R$	—	200	—	KHz
RF1 Center Frequency Range	f_{CEN}		1489	1540	1692	MHz
RF2 Center Frequency Range	f_{CEN}		1276	1365	1410	MHz
Tuning Range from f_{CEN}		Note: L_{EXT} ±10%	–6	—	6	%
RF1 VCO Pushing		Open loop	—	500	—	kHz/V
RF2 VCO Pushing			—	400	—	kHz/V
RF1 VCO Pulling		VSWR = 2:1, all phases, open loop	—	400	—	kHz_{PP}
RF2 VCO Pulling			—	100	—	kHz_{PP}
RF1 Phase Noise		1 MHz offset	—	–132	—	dBc/Hz
		3 MHz offset	—	–142	—	dBc/Hz
RF1 Integrated Phase Error		100 Hz to 100 kHz	—	1.0	—	deg rms
RF2 Phase Noise		1 MHz offset	—	–134	—	dBc/Hz
		3 MHz offset	—	–144	—	dBc/Hz
RF2 Integrated Phase Error		100 Hz to 100 kHz	—	1.0	—	deg rms
RF1 Harmonic Suppression		Second Harmonic	—	–26	—	dBc
RF2 Harmonic Suppression			—	–26	—	dBc
RFOUT Power Level		Z_L = 50 Ω	–7	–2	1	dBm
RF1 Reference Spurs		Offset = 200 kHz	—	–70	—	dBc
		Offset = 400 kHz	—	–75	—	dBc
		Offset = 600 kHz	—	–80	—	dBc
RF2 Reference Spurs		Offset = 200 kHz	—	–70	—	dBc
		Offset = 400 kHz	—	–75	—	dBc
		Offset = 600 kHz	—	–80	—	dBc
Powerup Request to Synthesizer Ready Time, RF1, RF2[2]	t_{pup}	Figures 4, 5	—	140	—	µs
Powerdown Request to Synthesizer Off Time[3]	t_{pdn}	Figures 4, 5	—	—	100	ns

Notes:
1. RF1 = 1.54 GHz, RF2 = 1.36 GHz for all parameters unless otherwise noted.
2. From powerup request ($\overline{PWDN}\uparrow$ or $\overline{SEN}\uparrow$ during a write of 1 to bit PDRB in Register 2) to RF synthesizers ready (settled to within 0.1 ppm frequency error). Typical settling time to 5 degrees phase error is 120 µs.
3. From powerdown request ($\overline{PWDN}\downarrow$, or $\overline{SEN}\uparrow$ during a write of 0 to bit PDRB in Register 2) to supply current equal to I_{PWDN}.

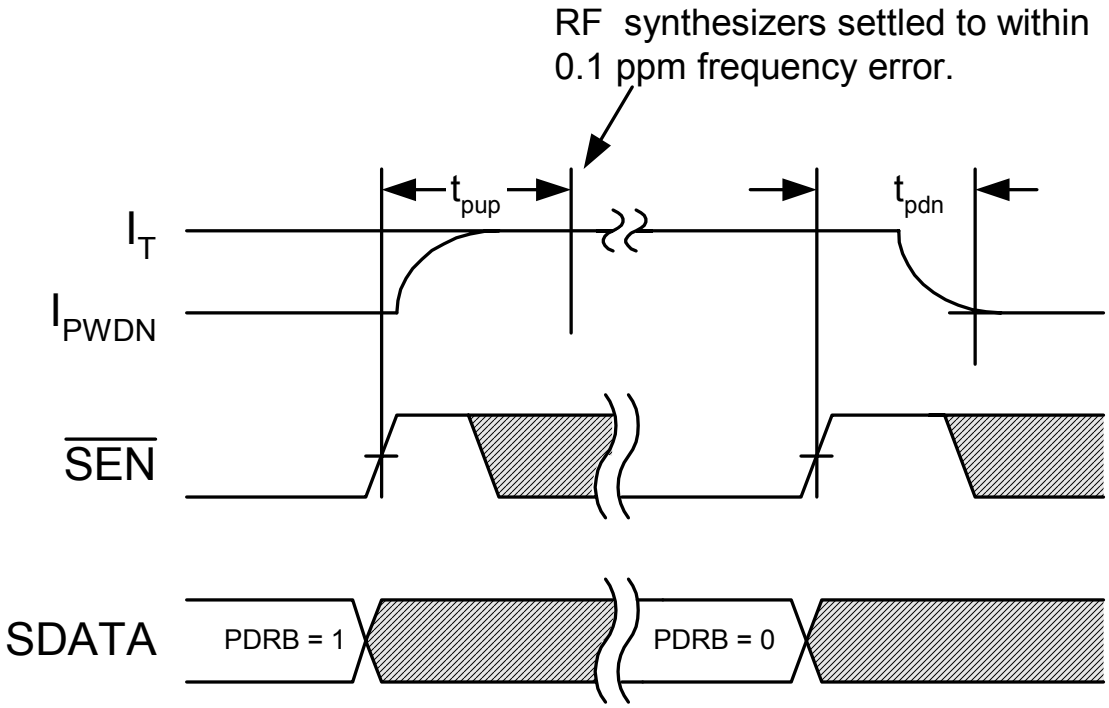


Figure 4. Software Power Management Timing Diagram

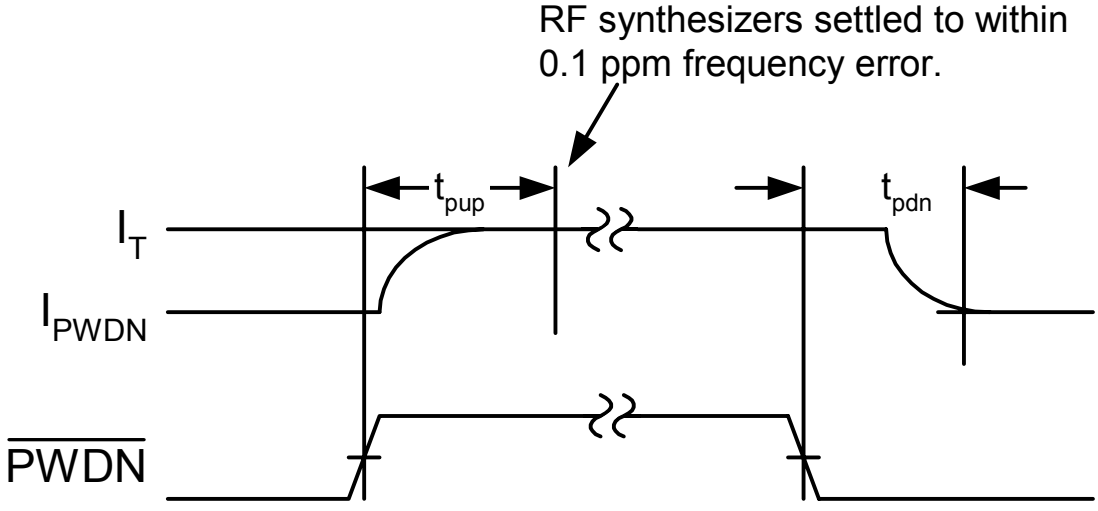


Figure 5. Hardware Power Management Timing Diagram

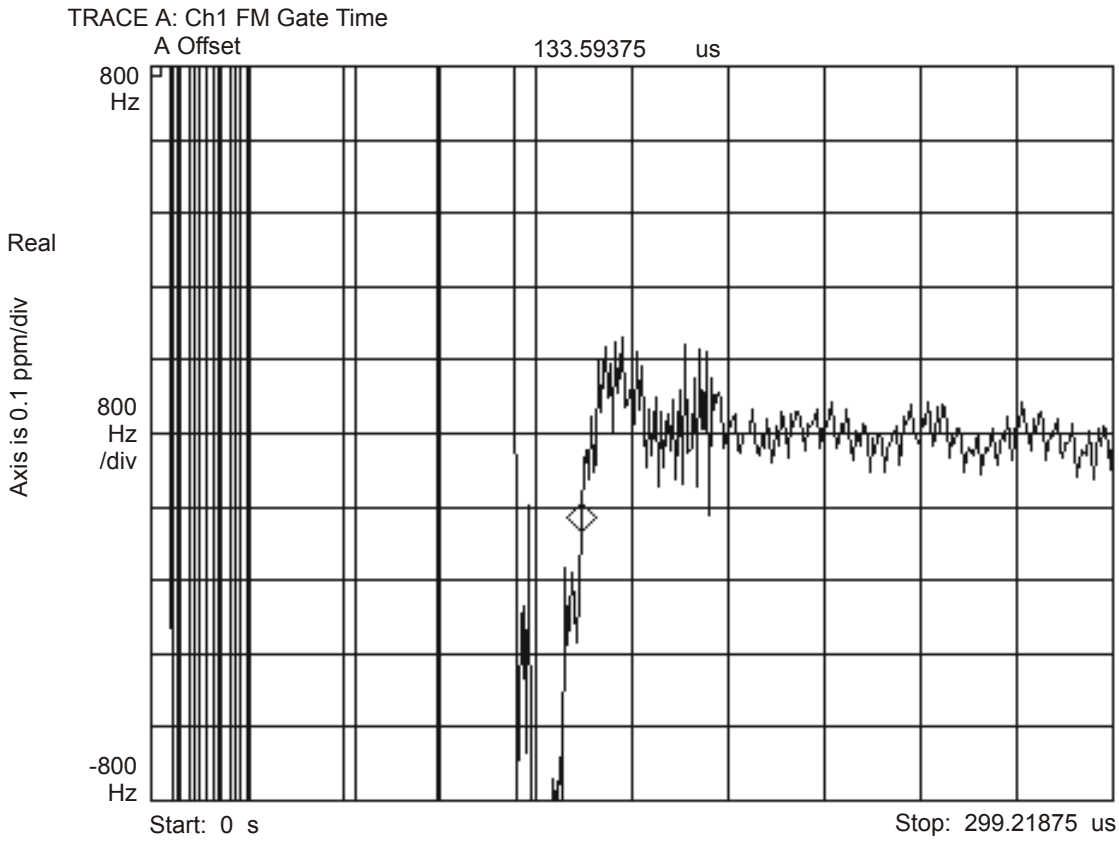


Figure 6. Typical Transient Response RF1 at 1.6 GHz with 200 kHz Phase Detector Update Frequency

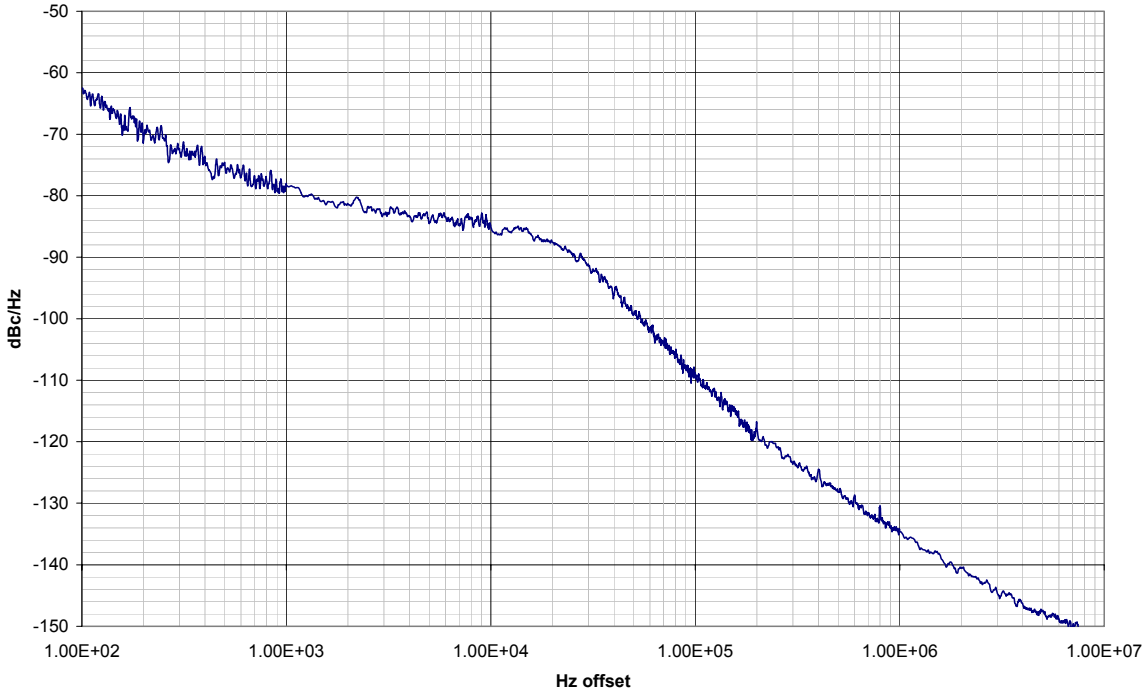


Figure 7. Typical RF1 Phase Noise at 1.54 GHz with 200 kHz Phase Detector Update Frequency

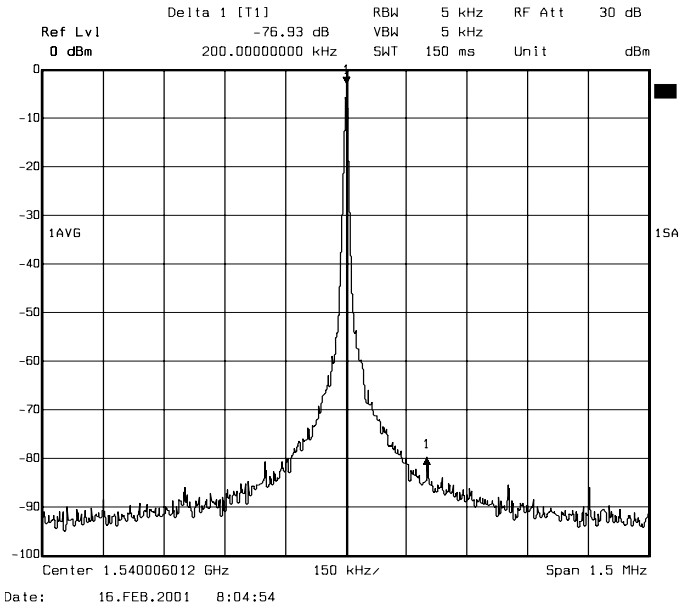


Figure 8. Typical RF1 Spurious Response at 1.54 GHz with 200 kHz Phase Detector Update Frequency

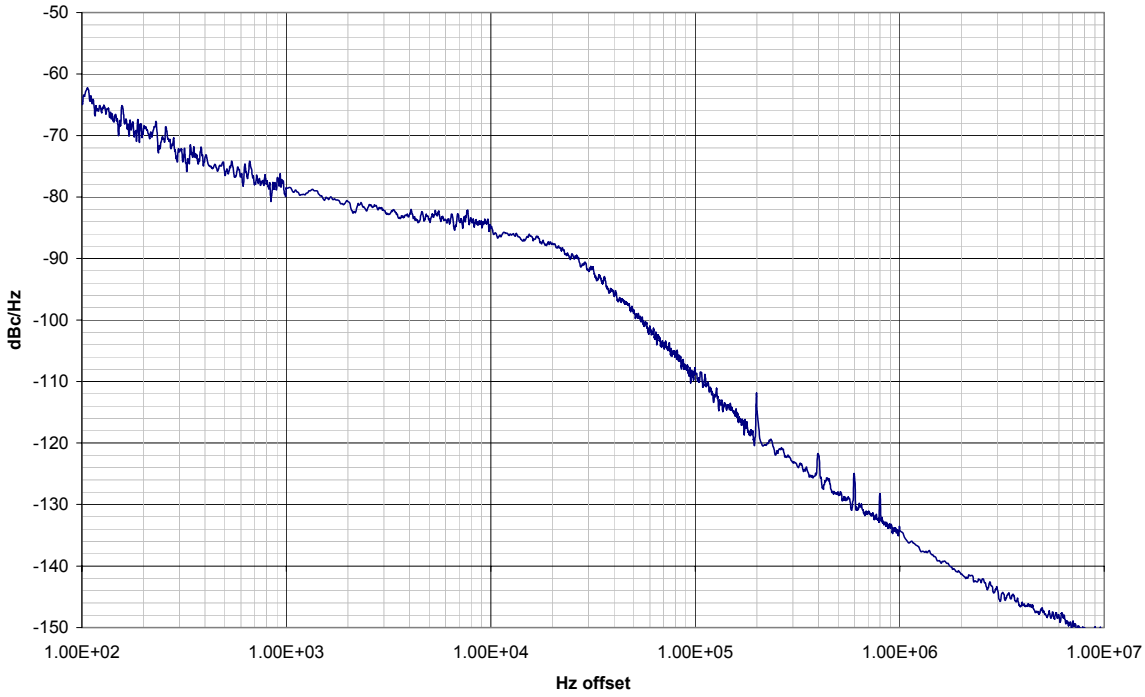


Figure 9. Typical RF2 Phase Noise at 1.36 GHz with 200 kHz Phase Detector Update Frequency

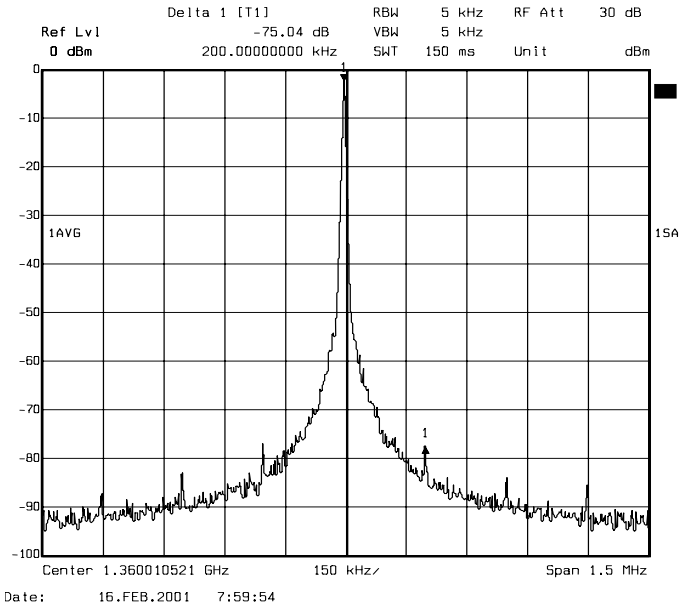


Figure 10. Typical RF2 Spurious Response at 1.36 GHz with 200 kHz Phase Detector Update Frequency

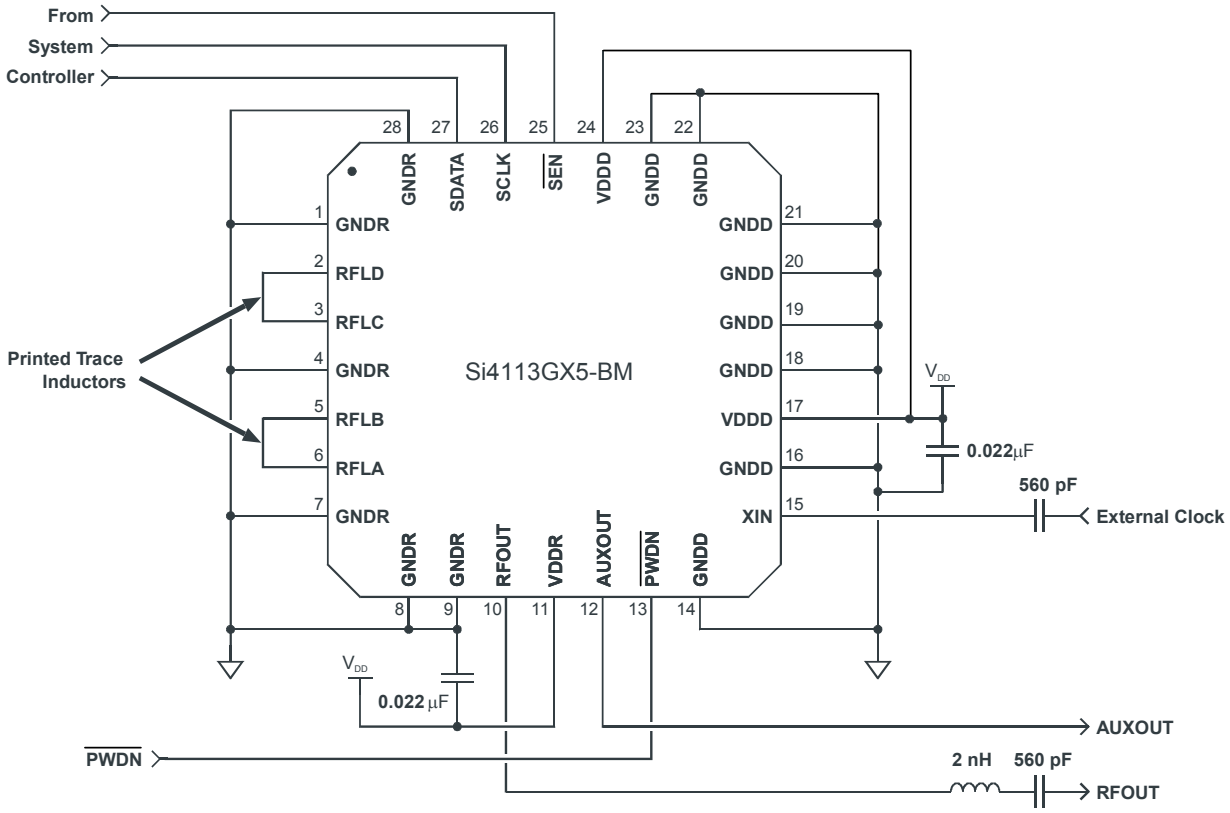


Figure 11. Typical Application Circuit: Si4113GX5-BM

Functional Description

The Si4113G-X5 is a monolithic integrated circuit that performs RF synthesis for dual and triple-band E-GSM 900, DCS 1800, and PCS 1900 applications. Optimized for use with the Infineon SMARTi and SMARTi+ GSM transceivers, its fast transient response also makes the Si4113G-X5 especially well suited to GPRS applications where channel switching and settling times are critical. This integrated circuit (IC), with a minimum number of external components, is all that is necessary to implement the frequency synthesis function.

The Si4113G-X5 has two complete phase-locked loops (PLLs) with integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4113G-X5 suitable for use in demanding wireless communications applications. Also integrated are phase detectors, loop filters, and reference dividers. The IC is programmed through a three-wire serial interface.

Two PLLs are provided for dual-band RF synthesis. One RF VCO (RF1) is optimized to have its center frequency set between 1489 and 1692 MHz, while the second RF VCO (RF2) is optimized to have its center frequency set between 1276 and 1410 MHz. Each PLL can adjust its output frequency by ±6% relative to its VCO center frequency.

The center frequency of each of the VCOs is set by connection of an external inductance. Inaccuracies in the value of the inductance are compensated for by the Si4113G-X5's proprietary self-tuning algorithm. This algorithm is initiated each time the PLL is powered up (by either the $\overline{\text{PWDN}}$ pin or by software) and/or each time a new output frequency is programmed.

The PLLs share a common output pin, so only one PLL is active at a time. Because the two VCOs can be set to have widely separated center frequencies, the RF output can be programmed to service different frequency bands, thus making the Si4113G-X5 ideal for use in triple-band cellular handsets.

The unique PLL architecture used in the Si4113G-X5 produces a transient response that is superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

Serial Interface

A timing diagram for the serial interface is shown in Figure 2 on page 7. Figure 3 on page 7 shows the format of the serial word.

The Si4113G-X5 is programmed serially with 22-bit words comprised of 18-bit data fields and 4-bit address fields. When the serial interface is enabled (i.e., when $\overline{\text{SEN}}$ is low) data and address bits on the SDATA pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of $\overline{\text{SEN}}$ into the internal data register addressed in the address field. The serial interface is disabled when $\overline{\text{SEN}}$ is high.

Table 9 on page 18 summarizes the data register functions and addresses. The internal shift register ignores leading bits before the 22 required bits.

Setting the VCO Center Frequencies

The PLLs can adjust the output frequencies ±6% with respect to their VCO center frequencies. Each center frequency is established by the value of an external inductance connected to the respective VCO. Manufacturing tolerances of ±10% for the external inductances are acceptable. The Si4113G-X5 compensates for inaccuracies in each inductance by executing a self-tuning algorithm after PLL powerup or after a change in the programmed output frequency.

Because the total tank inductance is in the low nH range, the inductance of the package needs to be considered in determining the correct external inductance. The total inductance (L_{TOT}) presented to each VCO is the sum of the external inductance (L_{EXT}) and the package inductance (L_{PKG}). Each VCO has a nominal capacitance (C_{NOM}) in parallel with the total inductance, and the center frequency is as follows:

$$f_{CEN} = \frac{1}{2\pi\sqrt{L_{TOT} \times C_{NOM}}}$$

or

$$f_{CEN} = \frac{1}{2\pi\sqrt{(L_{PKG} + L_{EXT}) \times C_{NOM}}}$$

Table 6 summarizes these characteristics for each VCO.

Table 6. Si4113GX5-BM VCO Characteristics

VCO	F_{CEN} Range (MHz)		C_{NOM} (pF)	L_{PKG} (nH)	L_{EXT} Range (nH)	
	Min	Max			Min	Max
RF1	1489	1692	4.3	1.5	0.56	1.16
RF2	1276	1410	4.8	1.5	1.15	1.74

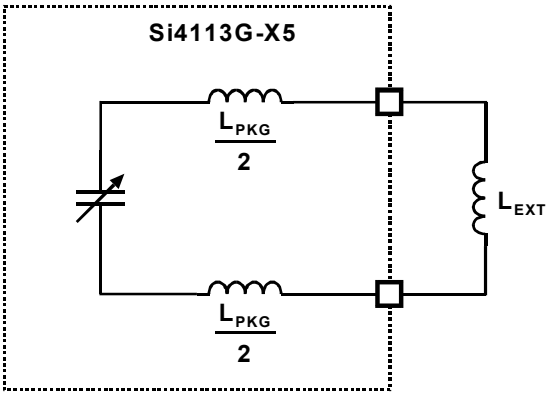


Figure 12. External Inductance Connection

In most cases, particularly for the RF VCOs, the requisite value of the external inductance is small enough to allow a PC board trace to be utilized. For more information, please refer to Application Note 31.

Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately after powerup of a PLL or, if the PLL is already powered, after a change in its programmed output frequency. This algorithm attempts to tune the VCO so that its free-running frequency is near the required output frequency. By doing so, the algorithm compensates for manufacturing tolerance errors in the value of the external inductance connected to the VCO. It also reduces the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

After self-tuning, the PLL controls the VCO oscillation frequency. The PLL will complete frequency locking to eliminate any remaining frequency error. Thereafter, it maintains frequency-lock, compensating for effects caused by temperature and supply voltage variations.

The Si4113G-X5's self-tuning algorithm compensates for component value errors at any temperature within the specified temperature range. However, the ability of the PLL to compensate for drift in component values that occur AFTER self-tuning is limited. For external inductances with temperature coefficients around ±150 ppm/°C, the PLL can maintain lock for changes in temperature of approximately ±30 °C.

Applications where the PLL is regularly powered down or switched between channels minimize or eliminate the potential effects of temperature drift because the VCO is re-tuned when it is powered up or when a new frequency is programmed. In applications where the ambient temperature can drift substantially after self-tuning, it might be necessary to monitor the LDETB (lock-detect bar) signal on the AUXOUT pin to determine the locking state of the PLL. (See "Auxiliary Output (AUXOUT)" on page 17 for how to select LDETB.)

The LDETB signal is low after self-tuning but rises when the PLL nears the limit of its compensation range (LDETB also is high when either PLL is executing the self-tuning algorithm). The output frequency is locked when LDETB goes high, but the PLL eventually loses lock if the temperature continues to drift in the same direction. Therefore, if LDETB goes high the RF PLLs should be re-tuned by initiating the self-tuning algorithm.

Output Frequencies

The RF output frequencies are set by programming the N-Divider registers. Each RF PLL has its own N register and can be programmed independently. Programming the N-Divider register for either RF1 or RF2 automatically selects the associated output. Either PLL R-divider option can be programmed to R = 65 or R = 130 to yield a 200 kHz phase detector update rate with either a 13 or 26 MHz reference frequency.

The reference frequency on the XIN pin is divided by R and this signal is the input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by N. The PLL works to make these frequencies equal after an initial transient:

$$\frac{f_{OUT}}{N} = \frac{f_{REF}}{65}$$

or

$$f_{OUT} = \frac{N}{65} \times f_{REF}$$

For XIN = 13 MHz this simplifies to the following:

$$f_{OUT} = N \times 200\ kHz$$

The integer N is set by programming the RF1 N-Divider register (Register 3) and the RF2 N-Divider register (Register 4).

Each N divider is implemented as a conventional high speed divider. That is, it consists of a dual-modulus prescaler, a swallow counter, and a lower speed synchronous counter. However, the calculation of these values is done automatically. Only the appropriate N value must be programmed.

SMARTi+ Frequency Plan

The Infineon SMARTi+ transceiver requires an LO range of 1285–1630 MHz for triple-band operation. The Si4113G-X5 can generate this range of frequencies using both RF1 and RF2 oscillators.

Figure 13 illustrates the recommended partition between the two oscillators. The total frequency range is divided between the two oscillators such that each must tune only ±6% from its center frequency. This frequency plan maximizes the amount of tuning range available to offset inductor tolerances for each oscillator.

These two oscillators are internally multiplexed to one output pin, RFOUT. This eliminates the need for any external switching to support all bands. The handset's system software controls which oscillator is active by writing N-values to either the RF1 or RF2 N-divider registers. N-values for frequencies of 1285–1447 MHz should be written to the RF2 N register (Register 4), and values for frequencies of 1448–1630 MHz to the RF1 N register (Register 3). This is summarized in Table 7.

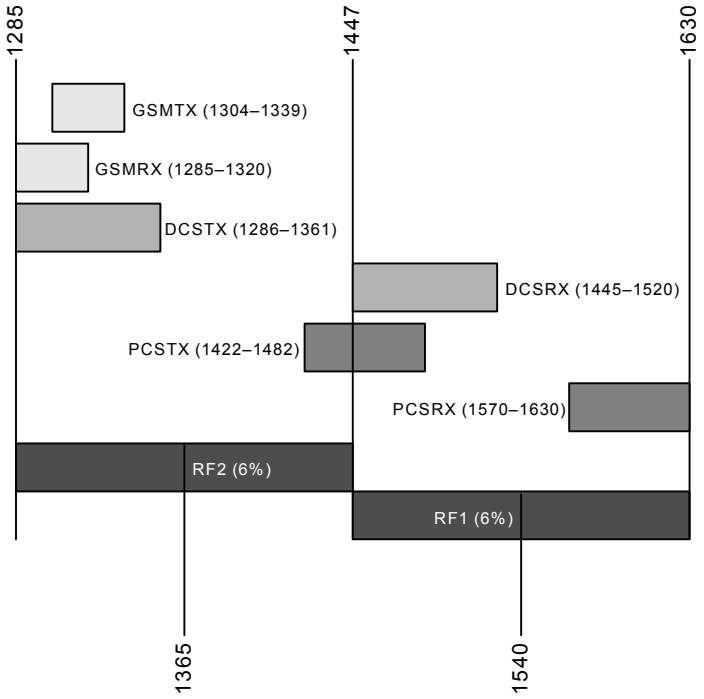


Figure 13. SMARTi+ Triple-Band LO Frequency Range Partitioned Between RF1 and RF2

Table 7. LO Configuration for Triple-Band SMARTi+ Frequency Plan

LO Frequency (MHz)	Center Frequency (MHz)	N-Divider Value (200 kHz phase detector)	Si4113G-X5 Oscillator	External Tuning Inductance/Pins (L_{EXT})
1285.0–1447.8	1365	6425–7239	RF2	1.332 nH/RFLC-RFLD
1448.0–1630.0	1540	7240–8150	RF1	0.984 nH/RFLA-RFLB

PLL Loop Dynamics

The transient response for each PLL is optimized for a GSM application. VCO gain, phase detector gain, and loop filter characteristics are not programmable.

The settling time for each PLL is directly proportional to its phase detector update period Tϕ (Tϕ equals 1/fϕ). For a GSM application with a 13 MHz reference frequency, the PLL's Tϕ = 5 μS. During the first 6.5 update periods, the Si4113G-X5 executes the self-tuning algorithm. Thereafter, the PLL controls the output frequency. Because of the unique architecture of the Si4113G-X5 PLLs, the time required to settle the output frequency to 0.1 ppm error is approximately 21 update periods. Thus, the total time after powerup or a change in programmed frequency until the synthesized frequency is well settled (including time for self-tuning) is around 28 update periods or 140 μS.

RF Outputs (RFOUT)

The RFOUT pin is driven by an amplifier that buffers the output pin from the RF VCOs, and must be coupled to its load through an ac coupling capacitor. The amplifier receives its input from either the RF1 or RF2 VCO, depending upon which N-Divider register was last written. For example, programming the N-Divider register for RF1 automatically selects the RF1 VCO output.

A matching network is required to maximize power delivered into a 50 Ω load. The network consists of a 2 nH series inductance, which can be realized with a PC board trace, connected between the RFOUT pin and the ac coupling capacitor. The network provides an adequate match for both the RF1 and RF2 frequency bands and also filters the output signal to reduce harmonic distortion. A 50 Ω load is not required for proper operation of the Si4113G-X5. Depending on transceiver requirements, the matching network may not be needed. See Figure 14.

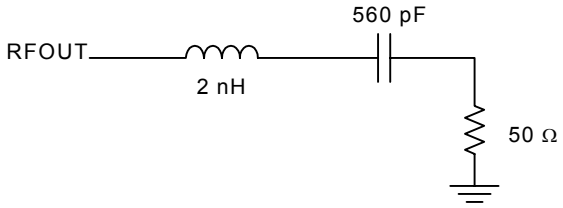


Figure 14. RFOUT 50 Ω Test Circuit

Reference Frequency Amplifier

The Si4113G-X5 provides a reference frequency amplifier. If the driving signal has CMOS levels it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be ac coupled to the XIN pin through a 100 pF capacitor.

Powerdown Modes

Table 8 summarizes the powerdown functionality. The Si4113G-X5 can be powered down by taking the $\overline{\text{PWDN}}$ pin low or by setting bits in the Powerdown register (Register 1). When the $\overline{\text{PWDN}}$ pin is low, the Si4113G-X5 is powered down regardless of the Powerdown register settings. When the $\overline{\text{PWDN}}$ pin is high, power management is under control of the Powerdown register bits.

Table 8. Powerdown Configuration

$\overline{\text{PWDN}}$ Pin	PDRB	Reference Frequency Amplifier	RF Circuitry
$\overline{\text{PWDN}}$ = 0	x	OFF	OFF
$\overline{\text{PWDN}}$ = 1	0	OFF	OFF
	1	ON	ON

Auxiliary Output (AUXOUT)

The signal appearing on AUXOUT is selected by setting the AUXSEL bits in the Main Configuration register (Register 0).

The LDETB signal can be selected by setting the AUXSEL bits to 011. This signal can be used to indicate that the PLL is about to lose lock due to excessive ambient temperature drift and should be re-tuned.

Control Registers

Table 9. Register Summary

Register	Name	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Main Configuration	0	0	0	0	AUXSEL [1:0]		0	0	0	0	0	RDIV	0	0	0	0	1	0
1	Reserved																		
2	Powerdown	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDRB
3	RF1 N Divider	N_{RF1}[17:0]																	
4	RF2 N Divider	0	N_{RF2}[16:0]																
5	Reserved																		
. . .																			
15	Reserved																		

Note: Registers 1 and 5–15 are reserved. Writes to these registers may result in unpredictable behavior. Any register not listed here is reserved and should not be written.

Register 0. Main Configuration Address Field = A[3:0] = 0000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	AUXSEL [1:0]		0	0	0	0	0	RDIV	0	0	0	0	1	0

Bit	Name	Function
17:14	Reserved	Program to zero.
13:12	AUXSEL[1:0]	**Auxiliary Output Pin Definition.** 00 = Reserved. 01 = Force output low. 10 = Reserved. 11 = Lock Detect (LDETB).
11:7	Reserved	Program to zero.
6	RDIV	**R Divider Selector.** 0 = ÷ 65. 1 = ÷ 130.
5:2	Reserved	Program to zero.
1	Reserved	Program to one.
0	Reserved	Program to zero.

Register 2. Powerdown Address Field (A[3:0]) = 0010

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDRB

Bit	Name	Function
17:1	Reserved	Program to zero.
0	PDRB	**Powerdown RF Synthesizer.** 0 = RF synthesizer powered down. 1 = RF synthesizer on.

Register 3. RF1 N Divider Address Field (A[3:0]) = 0011

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_{RF1}[17:0]																	

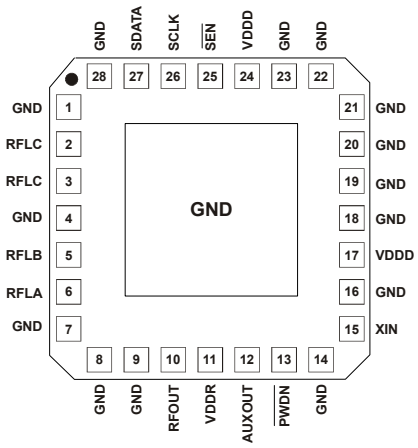
Bit	Name	Function
17:0	N_{RF1}[17:0]	**N Divider for RF1 Synthesizer.**

Register 4. RF2 N Divider Address Field = A[3:0] = 0100

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	N_{RF2}[16:0]																

Bit	Name	Function
17	Reserved	Program to zero.
16:0	N_{RF2}[16:0]	**N Divider for RF2 Synthesizer.**

Pin Descriptions: Si4113GX5-BM



Pin Number(s)	Name	Description
1, 4, 7–9, 14, 16, 18–23, 28	GND	Common ground
2, 3	RFLC, RFLD	Pins for inductor connection and digital RF2 VCO
5,6	RFLA, RFLB	Pins for inductor connection to RF1 VCO
10	RFOUT	Radio frequency (RF) output of the selected RF VCO
11	VDDR	Supply voltage for the RF analog circuitry
12	AUXOUT	Auxiliary output
13	$\overline{\text{PWDN}}$	Powerdown input pin
15	XIN	Reference frequency amplifier input
17, 24	VDDD	Supply voltage for digital circuitry
25	$\overline{\text{SEN}}$	Enable serial port input
26	SCLK	Serial clock input
27	SDATA	Serial data input

Ordering Guide

Ordering Part Number	Description	Operating Temperature
Si4113GX5-BM	Dual RF Synthesizer	–20 to 85 °C

Package Outline: Si4113GX5-BM

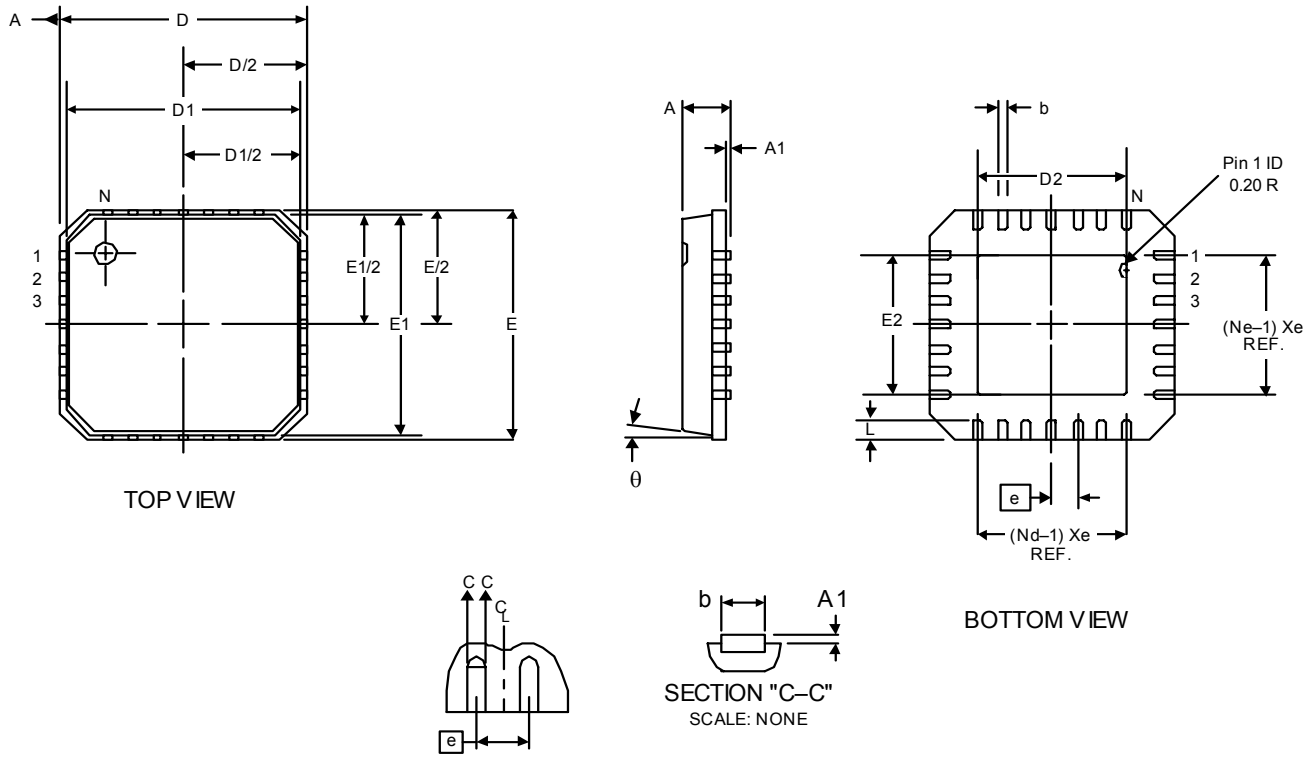


Figure 15. 28-Pin Micro Leadframe Package (MLP)

Table 10. Package Dimensions

Controlling Dimension: mm

Symbol	Millimeters		
	Min	Nom	Max
A	—	0.90	1.00
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D	5.00 BSC		
D1	4.75 BSC		
E	5.00 BSC		
E1	4.75 BSC		
N	28		
Nd	7		
Ne	7		
e	0.50 BSC		
L	0.50	0.60	0.75
θ			12°

Document Changes

Revision 0.4 to Revision 1.0

- Removed all preliminary banners and preliminary disclaimers.
- Updated RF2 spurious specifications in Table 5.

NOTES:

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