SILICON LABORATORIES

Si530

PRELIMINARY DATA SHEET

CRYSTAL OSCILLATOR (XO) (10 MHZ TO 1.4 GHZ)

Features

- Available with any-rate output frequencies from 10 MHz to 945 MHz and selected frequencies to 1.4 GHz
- Industry-standard 7x5 mm package
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3x better frequency stability than SAW-based oscillators
- 3rd generation DSPLL® with superior jitter performance
- Internal fixed crystal frequency ensures high reliability and low aging
- Lead-free/RoHS-compliant

Ordering Information:

See page 7.

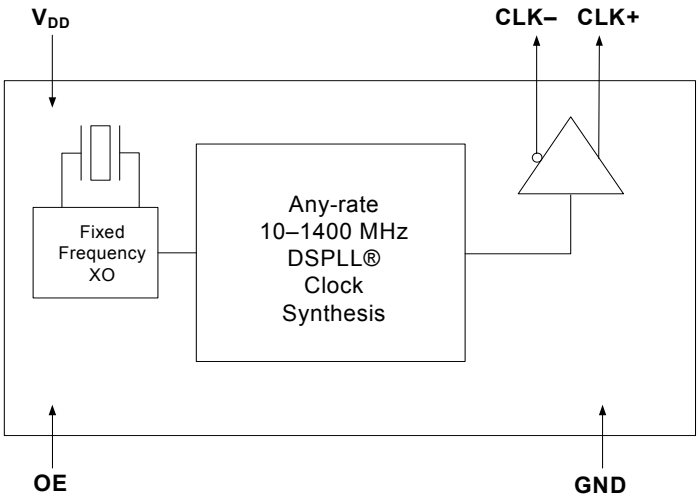
Applications

- Test and measurement equipment
- xDSL
- 10 GbE LAN/WAN
- Low-jitter clock generation
- Industrial electronics
- Clock and data recovery

Description

The Si530 XO utilizes Silicon Laboratories advanced DSPLL® circuitry to provide a low jitter clock at high frequencies. The Si530 is available with any-rate output frequency from 10 to 945 MHz and selected frequencies to 1400 MHz. Unlike a traditional XO, the crystal frequency inside the Si530 is fixed for a wide range of output frequencies. This IC based approach allows the crystal resonator to be optimized for superior frequency stability, reliability and mechanical integrity. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si530 IC based XO is factory configurable for a wide variety of user specifications including frequency, supply voltage and output format. Specific configurations are factory programmed into the Si530 at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

Functional Block Diagram



1. Electrical Specifications

Table 1. Si530 Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Frequency					
Nominal Frequency LVDS/CML/LVPECL CMOS	 10 10	 — —	 945 160	MHz	Specified at time of order by P/N. Also available in bands from 970 to 1134 MHz and 1213 to 1417 MHz.
Initial Accuracy	–1.5	—	+1.5	ppm	Measured at +25 °C at time of shipping.
Temperature Stability	–20 –50	— —	+20 +50	ppm	Option specified at time of order by P/N.
Aging	—	—	±10	ppm	Frequency drift over projected 15 year life.
Outputs					
Symmetry	45	—	55	%	Measured at: LVPECL: V_{DD} – 1.3 V (differential) LVDS: 1.25 V (differential) CMOS: V_{DD}/2
RMS Jitter for $F_{OUT} \geq$ 500 MHz 12 kHz to 20 MHz 50 kHz to 80 MHz	 — —	 0.27 0.30	 — —	ps	$F_{OUT} \geq$ 500 MHz Differential Modes: LVPECL/LVDS/CML
RMS Jitter for F_{OUT} of 125 to 500 MHz 12 kHz to 20 MHz	 —	 0.5	 —	ps	125 < F_{OUT} < 500 MHz Differential Modes: LVPECL/LVDS/CML
Period Jitter for $F_{OUT} \leq$160 MHz Peak-to-Peak RMS	 — —	 5 1	 — —	ps	Any output N = 1000 cycles
LVPECL Output Option mid-level swing (diff) swing (single-ended)	 V_{DD} – 1.42 1.1 0.5	 — — —	 V_{DD} – 1.25 1.9 0.93	 V V_{PP} V_{PP}	50 Ω to V_{DD} – 2.0 V
LVDS Output Option mid-level swing (diff)	 1.125 0.5	 1.2 0.7	 1.275 0.9	 V V_{PP}	R_{term} = 100 Ω (differential)
CML Output Option mid-level swing	 — 0.35	 V_{DD} – 0.36 0.425	 — 0.5	 V V_{PP}	R_{term} = 100 Ω (differential)

Table 1. Si530 Electrical Specifications (Continued)

Parameter	Min	Typ	Max	Units	Notes
CMOS Output Option V_{OH} V_{OL}	$0.8xV_{DD}$ —	— —	V_{DD} 0.4	V	C_L = 15 pF
Rise/Fall time	— — —	— — —	350 2 8	ps ns ns	CML/LVPECL/LVDS at 20%/80% CMOS with V_{DD} = 1.8 V & CL = 15 pF CMOS with V_{DD} = 3.3 V & CL = 15 pF
Inputs					
Voltage (V_{DD}) 3.3 V option 2.5 V option 1.8 V option	 2.97 2.25 1.71	 3.3 2.5 1.8	 3.63 2.75 1.89	V	Optional parameter specified by P/N
Current Output enabled TriState mode	 — —	 90 60	 — —	mA	
Output Enable V_{IH} V_{IL}	$0.75xV_{DD}$ —	— —	V_{DD} 0.5	V	

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage (V_{DD})	V_{DD}	–0.5 to +3.8	V
Storage Temperature	T_S	–55 to +125	°C

Table 3. Environmental Conditions

Parameter	Conditions/Test Method
Operating Temperature	–40 to +85 °C
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016

Table 4. Pinout

Pin	Symbol	LVDS/LVPECL/CML Function	CMOS Function
1	OE (CMOS only)	No connection	Tri-state output enable Disabled = logic “0” Enable = logic “1”
2	OE (LVPECL,LVDS,CML)	Tri-state output enable Disabled = logic “0” Enable = logic “1”	No connection
3	GND	Electrical and Case Ground	Electrical and Case Ground
4	CLK+	Oscillator Output	Oscillator Output
5	CLK–	Complementary output	No connection
6	V_{DD}	Power Supply Voltage	Power Supply Voltage

2. Outline Diagram and Suggested Pad Layout

Figure 1 illustrates the package details for the Si530. Table 5 lists the values for the dimensions shown in the illustration.

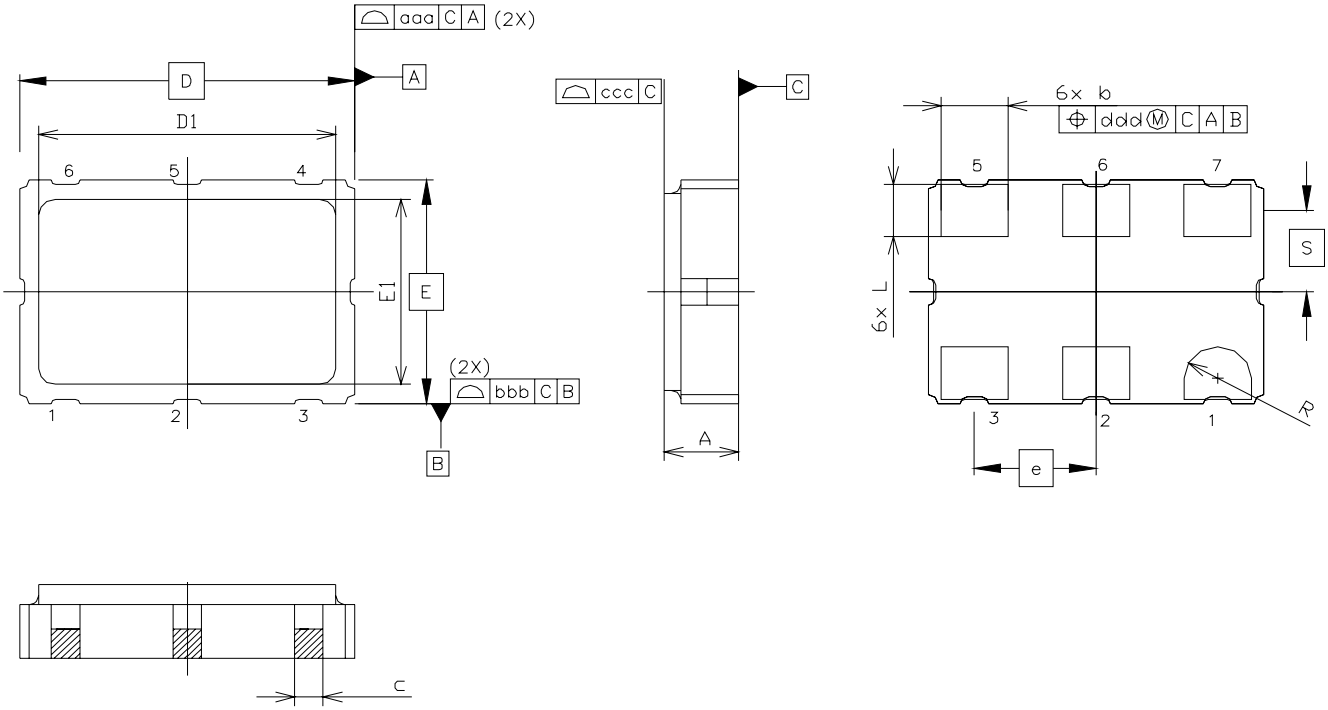


Figure 1. Si530 Outline Diagram

Table 5. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.45	1.65	1.85
b	1.2	1.4	1.6
c		0.60 TYP.	
D		7.00 BSC.	
D1	6.10	6.2	6.30
e		2.54 BSC.	
E		5.00 BSC.	
E1	4.30	4.40	4.50
L	1.07	1.27	1.47
S		1.815 BSC.	
R		0.7 REF.	
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

3. 6-Pin PCB Land Pattern

Figure 2 illustrates the 6-pin PCB land pattern for the Si530. Table 6 lists the values for the dimensions shown in the illustration.

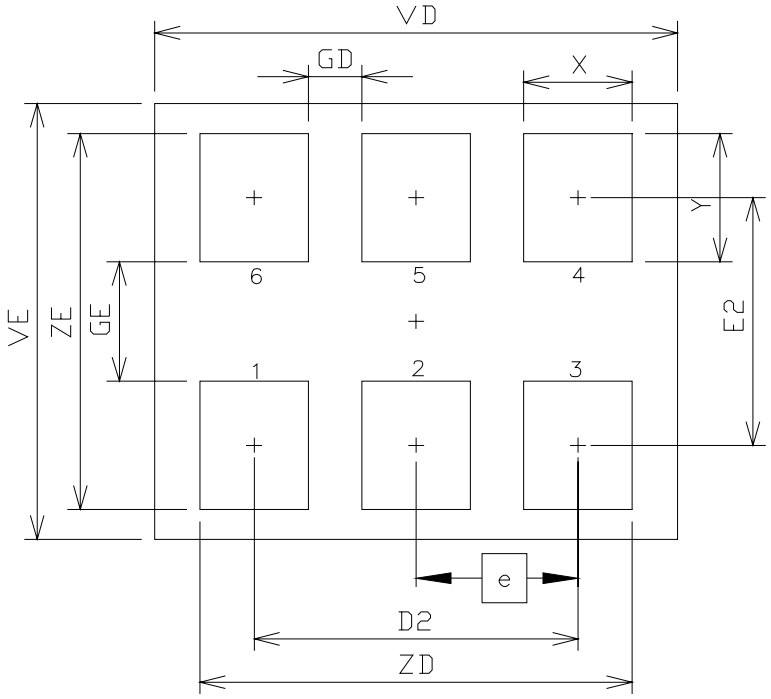


Figure 2. Si530 PCB Land Pattern

Table 6. PCB Land Pattern Dimensions (mm)

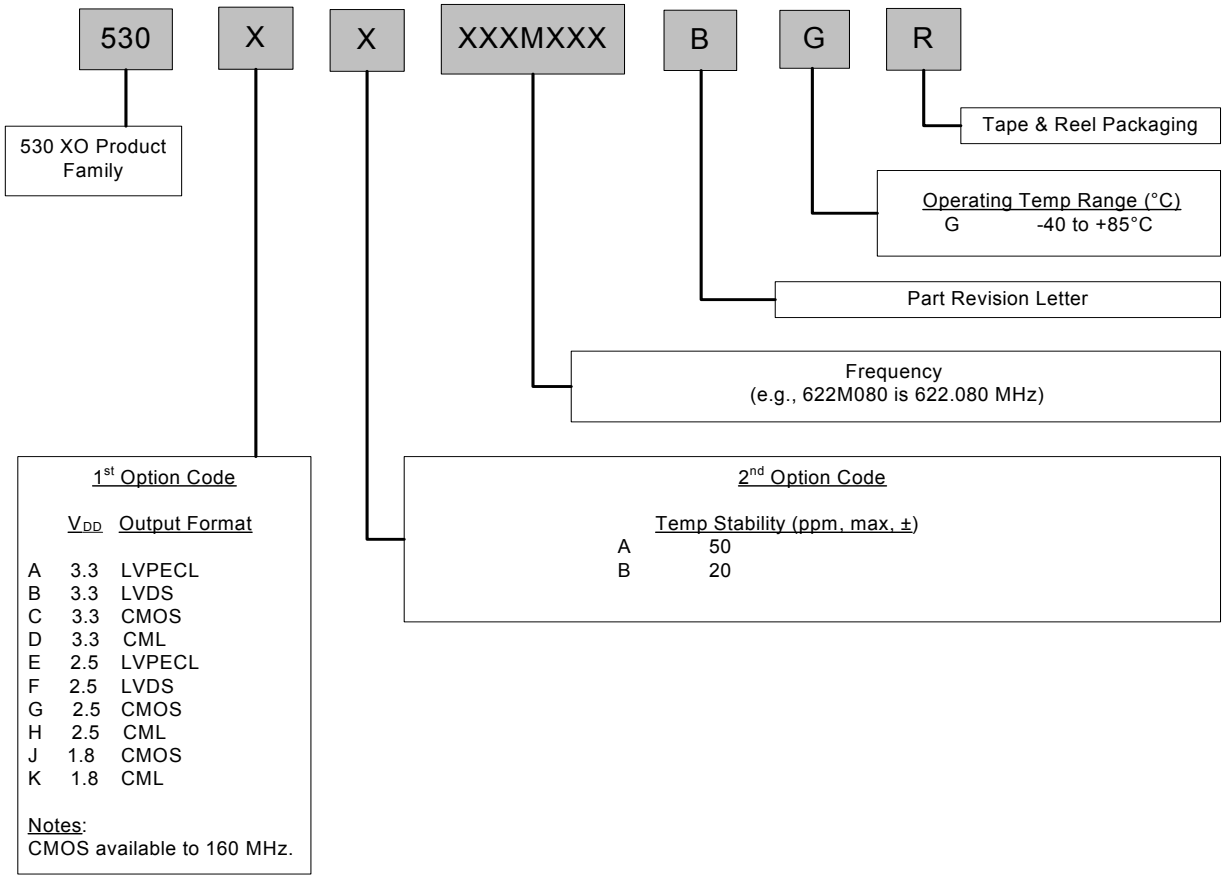
Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.15 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X	1.70 TYP	
Y	2.15 REF	
ZD	—	6.78
ZE	—	6.30

Notes:
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

4. Ordering Information

The Si530 XO was designed to support a variety of options including frequency, output format, and V_{DD}. Specific device configurations are programmed into the Si530 at time of shipment. Configurations can be specified using the part number configuration chart below. The Si530 XO series is supplied in an industry-standard 6-pad, 7x5 mm package.

Part numbers for the Si530 XO are determined by following configuration tables. Silicon Labs provides a Windows-based part number configuration tool to simplify this process. Refer to www.silabs.com/VCXO to access this tool and for further ordering instructions.



Example P/N: 530AB622M080BGR is a 7x5 XO in a 6 pad package. The frequency is 622.080 MHz, with a 3.3 V supply and PECL output. Stability is specifed as ± 20 ppm. The part is specified for -40 to +85 °C operation and will be shipped in tape and reel format.

CONTACT INFORMATION

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