SILICON LABORATORIES

Si554

PRELIMINARY DATA SHEET

QUAD FREQUENCY VCXO (10 MHZ TO 1.4 GHZ)

Features

- Available with any-rate output frequencies from 10 to 945 MHz and selected frequencies to 1.4 GHz
- Four selectable output frequencies
- Industry-standard 7x5 mm package
- Available CMOS, LVPECL, LVDS & CML outputs
- 3x better frequency stability than SAW-based oscillators
- 3rd generation DSPLL® with superior jitter performance
- Internal fixed crystal frequency ensures high reliability and low aging
- Lead-free/RoHS-compliant

Ordering Information:

See page 7.

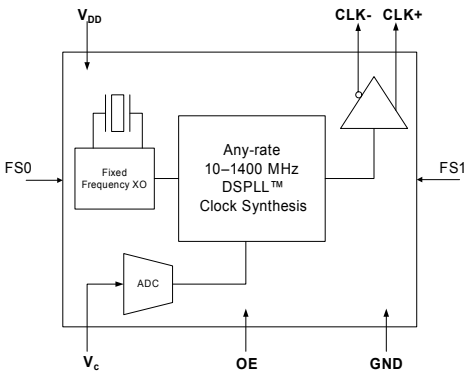
Applications

- SONET / SDH
- xDSL
- 10 GbE LAN / WAN
- Low jitter clock generation
- Optical Modules
- Test and Measurement

Description

The Si554 quad frequency VCXO utilizes Silicon Laboratories advanced DSPLL® circuitry to provide a very low jitter clock for all output frequencies. The Si554 is available with any-rate output frequency from 10 to 945 MHz and selected frequencies to 1400 MHz. Unlike traditional VCXOs where a different crystal is required for each output frequency, the Si554 uses one fixed crystal frequency to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to be optimized for superior frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments often found in communication systems. The Si554 IC-based VCXO is factory configurable for a wide variety of user specifications including frequency, supply voltage, and output format. Specific configurations are factory programmed into the Si554 at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

Functional Block Diagram



1. Electrical Specifications

Table 1. Si554 Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Frequency					
Nominal Frequency LVDS/CML/LVPECL CMOS	 10 10	 — —	 945 160	MHz	Specified at time of order by P/N. Also available in bands from 970 to 1134 MHz and 1213 to 1417 MHz.
Initial Accuracy	–1.5	—	1.5	ppm	Measured at +25 °C and $V_C = V_{DD}/2$ at time of shipping.
Temperature Stability	–20 –50 –100	— — —	+20 +50 +100	ppm	Selectable option by P/N. See Section 4. "Ordering Information" on page 7. Measured at $V_C = V_{DD}/2$.
Linearity BSL Incremental	 –5 –10	 ±1 ±5	 +5 +10	%	BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope determined with V_C ranging from 10 to 90% of V_{DD}.
Tuning Slope (kV) from 10 to 90% of V_{DD}	— — —	180 90 45	— — —	ppm/V	Positive slope; selectable option by part number. See Section 4. "Ordering Information" on page 7.
Modulation Bandwidth	—	10	—	kHz	
V_C Input Impedance	500	—	—	kΩ	
Absolute Pull Range (APR)	—	See Notes	—		
Aging	—	—	±10	ppm	Frequency drift over projected 15 year life.
Outputs					
Symmetry	45	—	55	%	LVPECL: V_{DD} – 1.3 V (differential) LVDS: 1.25 V (differential) CMOS: $V_{DD}/2$
RMS Jitter for $F_{OUT} \geq 500$ MHz Kv = 180 ppm/V 12 kHz to 20 MHz 50 kHz to 80 MHz Kv = 45, 90 ppm/V 12 kHz to 20 MHz 50 kHz to 80 MHz	 — — — —	 0.42 0.34 0.28 0.31	 — — — —	ps	$F_{OUT} \geq 500$ MHz Differential Modes: LVPECL/LVDS/CML

Table 1. Si554 Electrical Specifications (Continued)

Parameter	Min	Typ	Max	Units	Notes
RMS Jitter for F_{OUT} of 125 to 500 MHz 12 kHz to 20 MHz 50 kHz to 80 MHz	 — —	 0.61 0.52	 — —	ps	125 < F_{OUT} < 500 MHz Differential Modes: LVPECL/LVDS/CML
Period Jitter for $F_{OUT} \leq$ 160 MHz Peak-to-Peak RMS	 — —	 7 2	 — —	ps	Any output N = 1000 cycles
LVPECL Output Option mid-level swing (diff) swing (single-ended)	 V_{DD} – 1.42 1.1 0.5	 — — —	 V_{DD} – 1.25 1.9 0.93	 V V_{p-p} V_{p-p}	50 Ω to V_{DD} – 2.0 V
LVDS Output Option mid-level swing (diff)	 1.125 0.5	 1.2 0.7	 1.275 0.9	 V V_{p-p}	R_{term} = 100 Ω (differential)
CML Output Option mid-level swing	 — 0.35	 V_{DD} – 0.36 0.425	 — 0.5	 V V_{p-p}	Rterm = 100 Ω (differential)
CMOS Output Option V_{OH} V_{OL}	 0.8xV_{DD} —	 — —	 V_{DD} 0.4	 V	C_L = 15 pF
Rise/Fall time	— — —	— — —	350 2 8	ps ns ns	CML/LVPECL/LVDS at 20%/80% CMOS with V_{DD} = 1.8 V & CL = 15 pF CMOS with V_{DD} = 3.3 V & CL = 15 pF
Inputs					
Voltage (V_{DD}) 3.3 V option 2.5 V option 1.8 V option	 2.97 2.25 1.71	 3.3 2.5 1.8	 3.63 2.75 1.89	V	Optional parameter specified by P/N
Supply Current	—	90	—	mA	
Control Voltage (V_C)	0	—	V_{DD}	V	Tuning range for control voltage
Frequency Select[1:0] V_{IH} V_{IL}	 0.75 x V_{DD} 0	 — —	 V_{DD} 0.5	V	00 selects F0 01 selects F1 10 selects F2 11 selects F3
Output Enable V_{IH} V_{IL}	 0.75 x V_{DD} 0	 — —	 V_{DD} 0.5	V	

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Storage Temperature	T_S	–55 to +125	°C

Table 3. Environmental Conditions

Parameter	Conditions/ Test Method
Operating Temperature	–40 to +85 °C
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016

Table 4. Pinout

Pin	Symbol	Function
1	V_C	Control Voltage
2	OE	Output Enable Enabled when “1”
3	GND	Ground
4	CLK+	Output
5	CLK– (N/A for CMOS)	Complementary Output (N/C for CMOS)
6	V_{DD}	Power Suppy Voltage
7	FS[1]	Frequency Select MSB
8	FS[0]	Frequency Select LSB

2. Outline Diagram and Suggested Pad Layout

Figure 1 illustrates the package details for the Si554. Table 5 lists the values for the dimensions shown in the illustration.

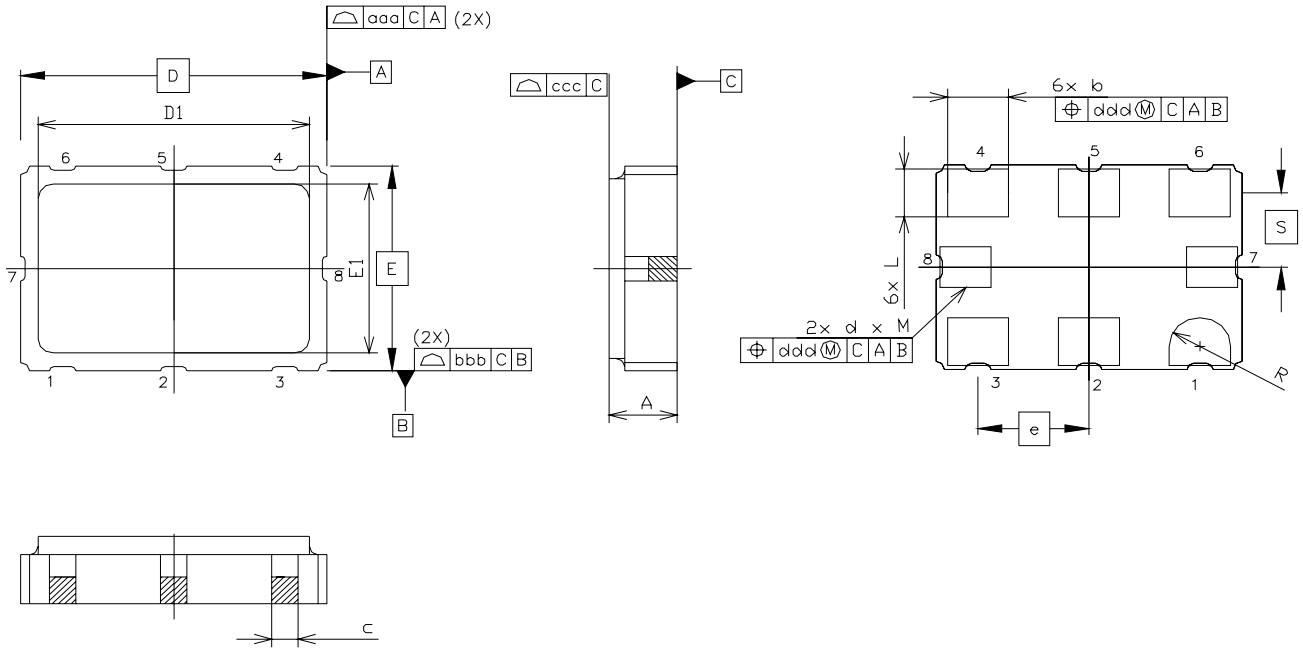


Figure 1. Si554 Outline Diagram

Table 5. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.45	1.65	1.85
b	1.2	1.4	1.6
c		0.60 TYP.	
d	0.97	1.17	1.37
D		7.00 BSC.	
D1	6.10	6.2	6.30
e		2.54 BSC.	
E		5.00 BSC.	
E1	4.30	4.40	4.50
L	1.07	1.27	1.47
M	0.8	1.0	1.2
S		1.815 BSC.	
R		0.7 REF.	
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

3. 8-Pin PCB Land Pattern

Figure 2 illustrates the 8-pin PCB land pattern for the Si554. Table 6 lists the values for the dimensions shown in the illustration.

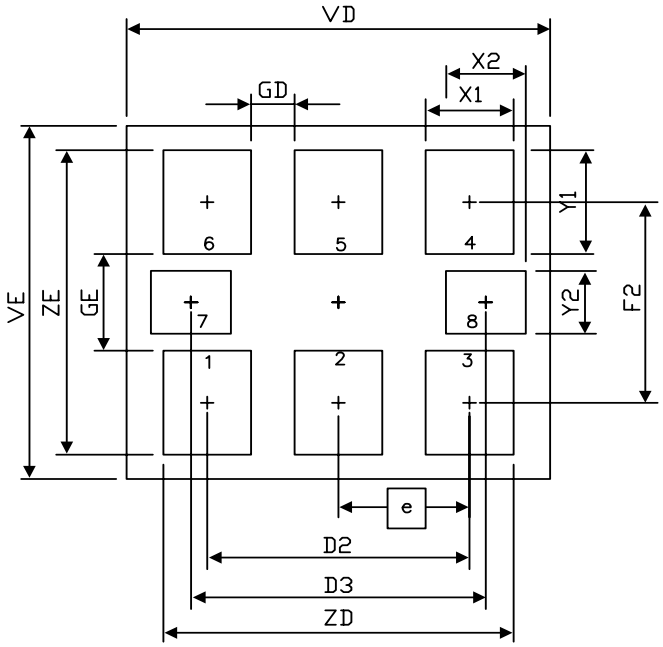


Figure 2. Si534 PCB Land Pattern

Table 6. PCB Land Pettern Dimensions (mm)

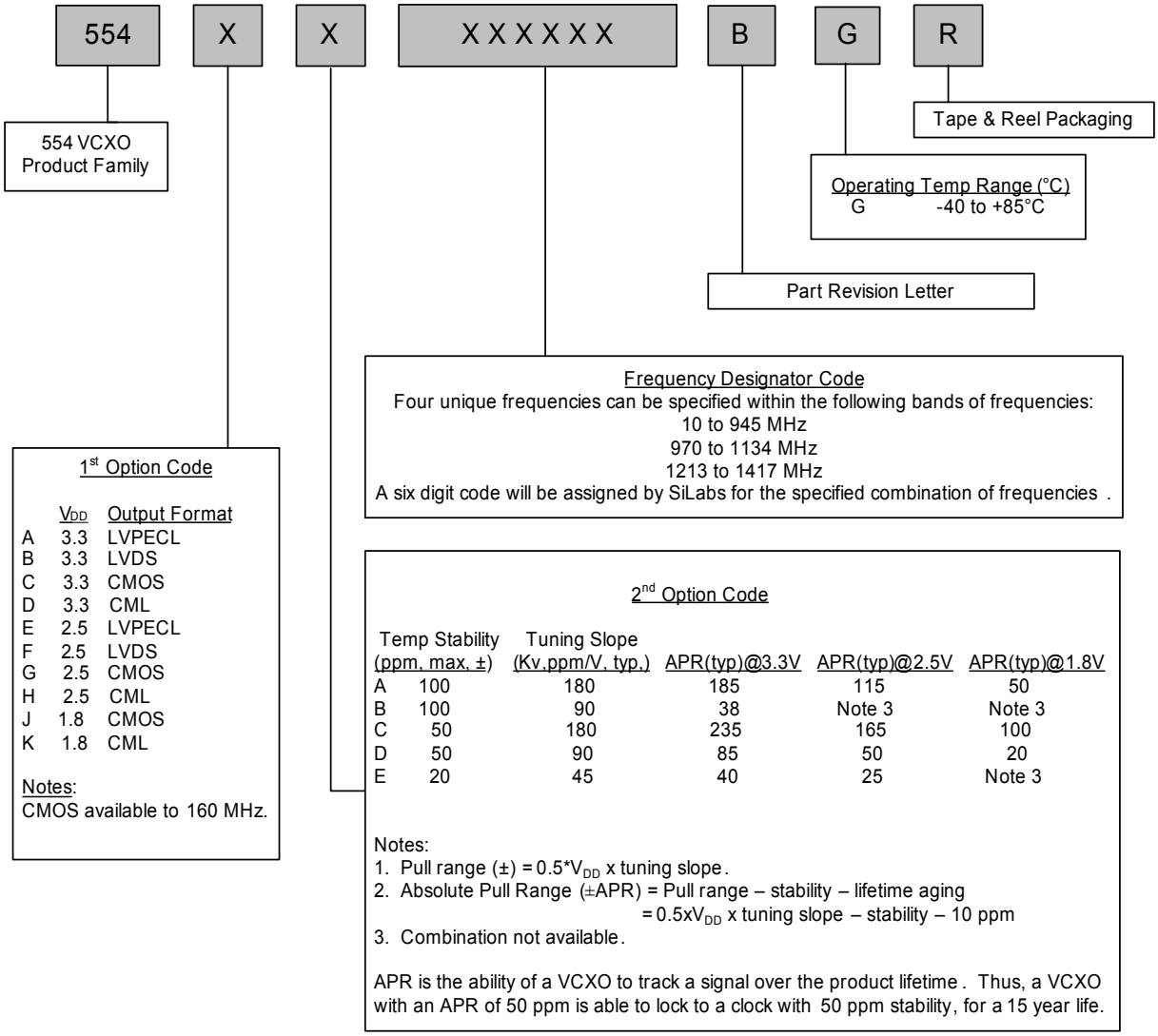
Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.20 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X1	1.70 TYP	
X2	1.545 TYP	
Y1	2.15 TYP	
X2	1.3 TYP	
ZD	—	6.78
ZE	—	6.30

Notes:
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design follows IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

4. Ordering Information

The Si554 was designed to support a variety of options including frequency, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si554 at time of shipment. A unique part number associated with these options and frequencies will be assigned. The Si554 Quad Frequency VCXO is provided in an 8-pad, 7x5 mm package

Part numbers for the Si554 Quad Frequency VCXO are determined by following configuration tables. Silicon Labs provides a Windows-based part number configuration tool to simplify this process. Refer to www.silabs.com/VCXO to access this tool and for further ordering instructions.



CONTACT INFORMATION

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: VCXOinfo@silabs.com
Internet: www.silabs.com