Preliminary Information

32-Channel High Voltage Sample and Hold Amplifier Array

Features

- ❑ 32 independent high voltage amplifiers
- ❑ 300V operating voltage
- ❑ 295V output voltage
- ❑ 2.2V/µs typical output slew rate
- ❑ Adjustable output current source limit
- ❑ Adjustable output current sink limit
- ❑ Internal closed loop gain of 72V/V
- ❑ 12MΩ feedback impedance
- ❑ Layout ideal for die applications

Application

- ❑ MEMS (microelctromechanical systems) driver
- ❑ Piezoelectric transducer driver
- ❑ Optical crosspoint switches (using MEMS technology)

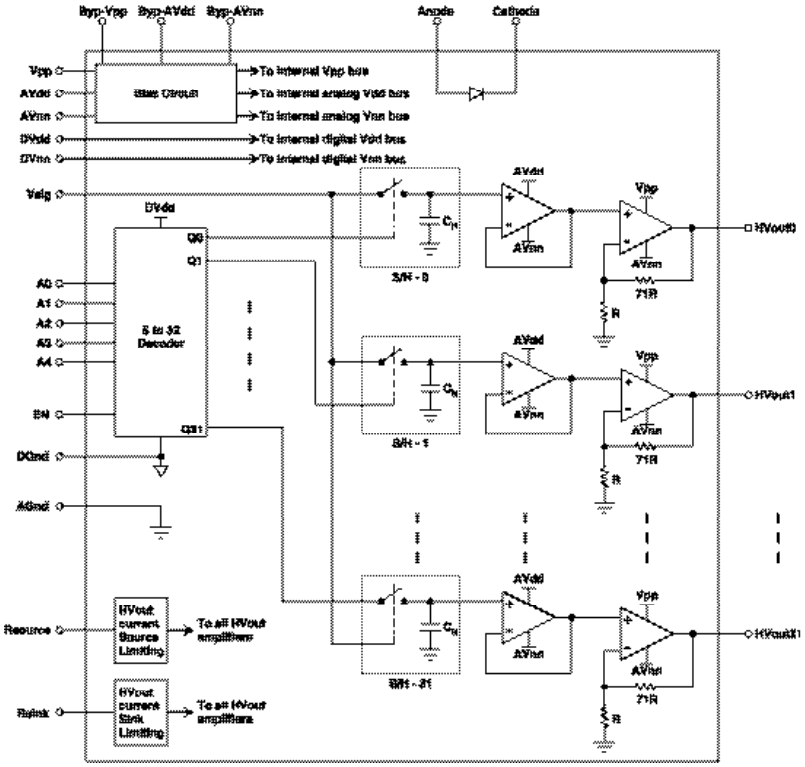
General Description

The Supertex HV257 is a 32-channel high voltage sample and hold amplifier array integrated circuit. It operates on a single high voltage supply, up to 300V, and two low voltage supplies, V_{DD} and V_{NN}.

All 32 sample and hold circuits share a common analog input, Vsig. The individual sample and hold circuits are selected by a 5 to 32 logic decoder. The sampled voltage on the holding capacitor is buffered by a low voltage amplifier and amplified by a high voltage amplifier with a closed loop gain of 72V/V. The internal closed loop gain is set for an input voltage range of 0V to 4.096V. The input voltage can be up to 5.0V, but the output will saturate. The maximum output voltage swing is 5V below the V_{PP} high voltage supply. The outputs can drive capacitive loads of up to 3000pF.

The maximum output source and sink current can be adjusted by using two external resistors. An external R_{SOURCE} resistor controls the maximum sourcing current and an external R_{SINK} resistor controls the maximum sinking current. The current limit is approximately 12.5V divided by the external resistor value. The setting is common for all 32 outputs. A low voltage silicon junction diode is made available to help monitor the die temperature.

Block Diagram



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Ordering Information

Device	Maximum Output Voltage	Nominal Closed Loop Gain	Package Options	
			100 Lead MQFP	Die
HV257	295V	72V/V	HV257FG	HV257X

Absolute Maximum Ratings*

V_{PP}, High voltage supply	310V
AV_{DD}, Analog low voltage positive supply	8.0V
DV_{DD}, Digital low voltage positive supply	8.0V
AV_{NN}, Analog low voltage negative supply	-7.0V
DV_{NN}, Digital low voltage negative supply	-7.0V
Logic input voltage	-0.5V to DV_{DD}
V_{IN}, Analog input signal	0V to 6.0V
Storage temperature range	-65∞C to 150°C
Maximum junction temperature	150°C

***Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.**

Electrical Characteristics (Over operating conditions unless otherwise noted.)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Operating Conditons						
V_{PP}	High voltage positive supply	125		300	V	
V_{DD}	Low voltage positive supply	6.0		7.5	V	
V_{NN}	Low voltage negative supply	-4.5		-6.5	V	
I_{PP}	V_{PP} supply current			0.8	mA	V_{PP}=300V, All HV_{OUT}=0V, No Load
I_{DD}	V_{DD} supply current			4.3	mA	V_{DD} = 6.0V to 7.5V
I_{NN}	V_{NN} supply current	-5.2			mA	V_{NN} = -4.5V to -6.5V
T_J	Junction temperature range	-10		125	°C	
High Voltage Amplifier						
HV_{OUT}	HV_{OUT} voltage swing	0		V_{PP}-5	V	
V_{INOS}	Input voltage range			±50	mV	Input referred.
SR	HV_{OUT} slew rate rise		2.2		V/µs	No Load
	HV_{OUT} slew rate fall		2.0		V/µs	No Load
BW	HV_{OUT} -3dB channel bandwidth		4.0		KHz	V_{PP}=300V
A_O	Open loop gain	70	100		dB	
A_V	Closed loop gain	68.4	72.0	75.6	V/V	
R_{FB}	Feedback resistance from HV_{OUT} to ground	9.6	12		MΩ	
C_{LOAD}	HV_{OUT} capacitive load	0		3000	pF	
I_{SOURCE}	HV_{OUT} sourcing current limiting range	385	550	715	µA	R_{SOURCE} = 25KΩ
I_{SINK}	HV_{OUT} sinking current limiting range	385	550	715	µA	R_{SINK} = 25KΩ
R_{SOURCE}	External resistance range for setting current source limit	25		250	KΩ	
R_{SINK}	External resistance range for setting current sink limit	25		250	KΩ	
CT_{DC}	DC channel to channel crosstalk	-80			dB	
PSRR	Power supply rejection ratio for V_{PP}, V_{DD}, and V_{NN}	-40			dB	

Sample and Hold

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Vped	Pedestal Voltage			TBD	mV	
Rsw	Sample and Hold Switch resistance		5.0	TBD	KΩ	
C_H	Samp and Hold capacitor		10	TBD	pF	
Rdroop	Droop rate during hold time relative to input			TBD	V/s	
Vsig	Input voltage range	0		5.0	V	

Logic Decoder

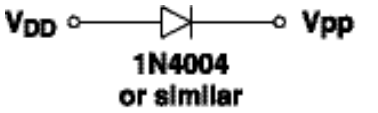
Symbol	Parameter	Min	Typ	Max	Units	Conditions
tsu	Set-up time-address to enable	75			ns	
th	Hold time-address to enable bar	75			ns	
Vih	Input logic high voltage	2.4		V_{DD}	V	
Vil	Input logic low voltage	0		1.2	V	
Iih	Input logic high current			1.0	µA	Vih = V_{DD}
Iil	Input logic low current	-1.0			µA	Vil = 0V

Diode

Symbol	Parameter	Min	Typ	Max	Units	Conditions
PIV	Peak inverse voltage			5.0	V	cathode to anode
V_F	Forward diode drop			0.8	V	If=2.0mA, anode to cathode
I_F	Forward diode current			2.0	mA	anode to cathode
T_C	V_F temperature coefficient		TBD		mV/°C	anode to cathode

Power Up/Down Sequence

The device can be damaged due to improper power up / down sequence. To prevent damage, please follow the acceptable power up /down sequences and add two external diodes as shown in the diagram below. The first diode is a high voltage diode across V_{PP} and V_{DD} where the anode of the diode is connected to V_{DD} and the cathode of the diode is connected to Vpp. Any low current high voltage diode such as a 1N4004 will be adequate. The second diode is a schottky diode across V_{NN} and DGnd where the anode of the schottky diode is connected to V_{NN} and the cathode is connected to DGnd. Any low current schottky diode such as a 1N5817 will be adequate.



Acceptable Power Up Sequences

1) V_{PP}	2) V_{NN}	3) V_{DD}	4) Inputs & Anode
1) V_{DD}	2) V_{NN}	3) V_{PP}	4) Inputs & Anode

Acceptable Power Down Sequences

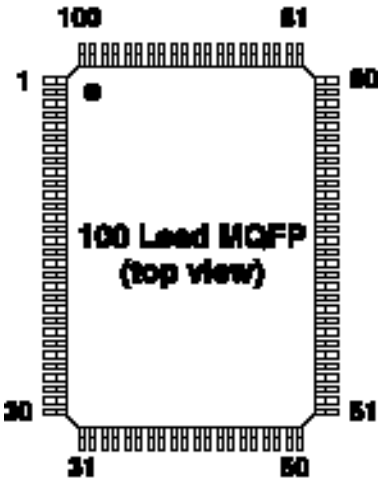
1) Inputs & Anode	2) V_{PP}	3) V_{DD}	4) V_{NN}
1) Inputs & Anode	2) V_{DD}	3) V_{NN}	4) V_{PP}

Truth Table

A4	A3	A2	A1	A0	EN	Selected S/H
L	L	L	L	L	H	0
L	L	L	L	H	H	1
L	L	L	H	L	H	2
L	L	L	H	H	H	3
⋮			⋮			⋮
H	H	H	L	H	H	29
H	H	H	H	L	H	30
H	H	H	H	H	H	31
X	X	X	X	X	L	All Open

Pin Description

V_{PP}	High voltage positive supply. There are two pads.
B_{YP}-V_{PP}	A low voltage 1.0 to 10nF decoupling capacitor across V_{PP} and B_{YP}-V_{PP} is required.
AV_{DD}	Analog low voltage positive supply. This should be at the same potential as DV_{DD}. There are two pads.
B_{YP}-AV_{DD}	A low voltage 1.0 to 10nF decoupling capacitor across AV_{DD} and B_{YP}-AV_{DD} is required.
AV_{NN}	Analog low voltage negative supply. This should be the same potential as DV_{NN}. There are two pads.
B_{YP}-AV_{NN}	A low voltage 1.0 to 10nF decoupling capacitor across AV_{NN} and B_{YP}-AV_{NN} is required.
DV_{DD}	Digital low voltage positive supply. This should be the same potential as AV_{DD}. There are two pads.
DV_{NN}	Digital low voltage negative supply. This should be the same potential as AV_{NN}. There are two pads.
DGND	Digital ground.
AGND	Analog ground. There are three pads. They need to be externally connected together.
A0 to A4	Decoder logic inputs. Addressed channel will close the sample and hold switch. Sample and hold switches for unaddressed channels are kept open.
EN	Active logic high input. Logic low will keep sample and hold switches open.
Vsig	Common input signal for all 32 sample and hold circuits.
R_{SOURCE}	External resistor from R_{SOURCE} to V_{NN} sets output current sourcing limit. Current limit is approximately 12.5V divided by Rsource resistor value.
R_{SINK}	External resistor from R_{SINK} to V_{NN} sets output current sinking limit. Current limit is approximately 12.5V divided by R_{SINK} resistor value.
Anode	Anode side of a low voltage silicon diode that can be used to monitor die temperature.
Cathode	Cathode side of a low voltage silicon diode that can be used to monitor die temperature.
$HV_{OUT}0$ to $HV_{OUT}31$	Amplifier outputs.



Pin #	Function
1	$HV_{OUT}31$
2	$HV_{OUT}30$
3	$HV_{OUT}29$
4	$HV_{OUT}28$
5	$HV_{OUT}27$
6	$HV_{OUT}26$
7	$HV_{OUT}25$
8	$HV_{OUT}24$
9	$HV_{OUT}23$
10	$HV_{OUT}22$
11	$HV_{OUT}21$
12	$HV_{OUT}20$
13	$HV_{OUT}19$
14	$HV_{OUT}18$
15	$HV_{OUT}17$
16	$HV_{OUT}16$
17	$HV_{OUT}15$
18	$HV_{OUT}14$
19	$HV_{OUT}13$
20	$HV_{OUT}12$
21	$HV_{OUT}11$
22	$HV_{OUT}10$
23	$HV_{OUT}9$
24	$HV_{OUT}8$
25	$HV_{OUT}7$

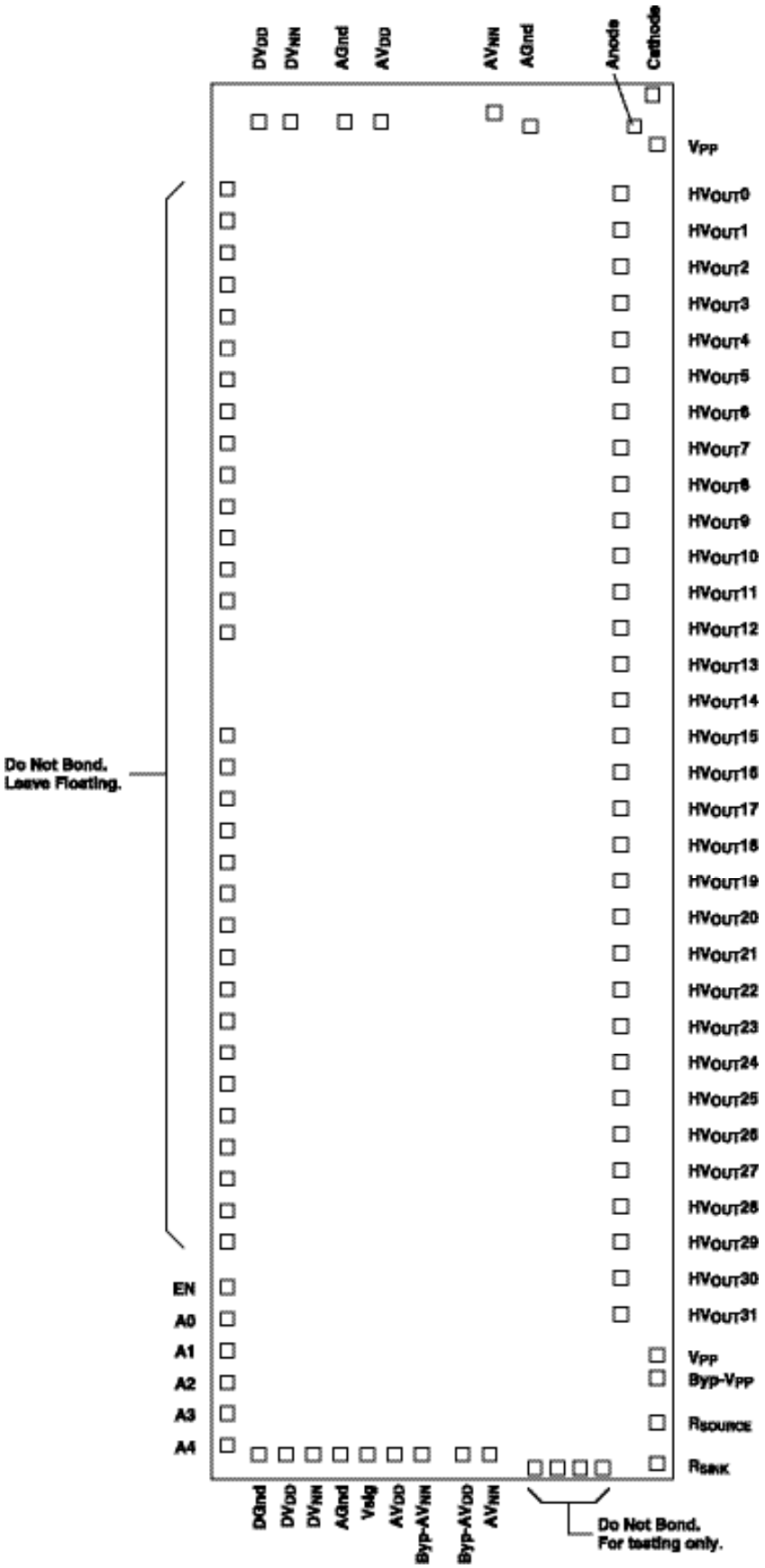
Pin #	Function
26	$HV_{OUT}6$
27	$HV_{OUT}5$
28	$HV_{OUT}4$
29	$HV_{OUT}3$
30	$HV_{OUT}2$
31	$HV_{OUT}1$
32	$HV_{OUT}0$
33	V_{PP}
34	NC
35	NC
36	Cathode
37	Anode
38	NC
39	AGnd
40	AV_{NN}
41	NC
42	AV_{DD}
43	AGnd
44	DV_{NN}
45	DV_{DD}
46	NC
47	NC
48	NC
49	NC
50	NC

Pin #	Function
51	NC
52	NC
53	NC
54	NC
55	NC
56	NC
57	NC
58	NC
59	NC
60	NC
61	NC
62	NC
63	NC
64	NC
65	NC
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	NC
75	NC

Pin #	Function
76	NC
77	NC
78	NC
79	NC
80	EN
81	A0
82	A1
83	A2
84	A3
85	A4
86	DGnd
87	DV_{DD}
88	DV_{NN}
89	AGnd
90	Vsig
91	AV_{DD}
92	Byp-AV_{NN}
93	Byp-AV_{DD}
94	AV_{NN}
95	NC
96	NC
97	R_{SINK}
98	R_{SOURCE}
99	Byp-V_{PP}
100	V_{PP}

NC=No Connect.

Pad Configuration (Not Drawn to Scale)



Pad Coordinates

Chip size: 17004µm x 5480µm
Center of die is (0,0)

Pad Name	X (µm)	Y (µm)
EN	6248.5	-2514.5
A0	6653.5	-2514.5
A1	7058.5	-2514.5
A2	7463.5	-2514.5
A3	7868.5	-2514.5
A4	8273.5	-2514.5
Dgnd	8320	-2150
DV_{DD}	8320	-1785.5
DV_{NN}	8320	-1485
Agnd	8300	-1185.5
Vsig	8300	-819.5
AV_{DD}	8300	-519.5
Byp_AV_{NN}	8300	-219.5
Byp_AV_{DD}	8300	295.5
AV_{NN}	8300	595.5
R_{SINK}	8340	2538
R_{SOURCE}	7860	2538
Byp_AV_{PP}	7313	2538
V_{PP}	7013	2538
$HV_{OUT}31$	6512.0	2129.5
$HV_{OUT}30$	6065.0	2129.5
$HV_{OUT}29$	5618.0	2129.5
$HV_{OUT}28$	5171.0	2129.5
$HV_{OUT}27$	4724.0	2129.5
$HV_{OUT}26$	4277.0	2129.5
$HV_{OUT}25$	3830.0	2129.5
$HV_{OUT}24$	3383.0	2129.5
$HV_{OUT}23$	2936.0	2129.5
$HV_{OUT}22$	2489.0	2129.5
$HV_{OUT}21$	2042.0	2129.5

Pad Name	X (µm)	Y (µm)
$HV_{OUT}20$	1595.0	2129.5
$HV_{OUT}19$	1148.0	2129.5
$HV_{OUT}18$	701.0	2129.5
$HV_{OUT}17$	254.0	2129.5
$HV_{OUT}16$	-193.0	2129.5
$HV_{OUT}15$	-640.0	2129.5
$HV_{OUT}14$	-1087.0	2129.5
$HV_{OUT}13$	-1534.0	2129.5
$HV_{OUT}12$	-1981.0	2129.5
$HV_{OUT}11$	-2428.0	2129.5
$HV_{OUT}10$	-2875.0	2129.5
$HV_{OUT}9$	-3322.0	2129.5
$HV_{OUT}8$	-3769.0	2129.5
$HV_{OUT}7$	-4216.0	2129.5
$HV_{OUT}6$	-4663.0	2129.5
$HV_{OUT}5$	-5110.0	2129.5
$HV_{OUT}4$	-5557.0	2129.5
$HV_{OUT}3$	-6004.0	2129.5
$HV_{OUT}2$	-6451.0	2129.5
$HV_{OUT}1$	-6898.0	2129.5
$HV_{OUT}0$	-7345.5	2129.5
V_{PP}	-7693.5	2536.5
Cathode	-8072.5	2488.5
Anode	-7803	2236.5
Agnd	-7825.5	725.5
AV_{NN}	-7921.5	425.5
AV_{DD}	-7837	-972.5
Agnd	-7817	-1390.5
DV_{NN}	-7823	-1779
DV_{DD}	-7823	-2080.5

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