

## 64-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

### Ordering Information

Device	Recommended Operating $V_{PP}$ Max	Package Options		
		80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	Die
HV3418	180V	HV3418DG	HV3418PG	HV3418X

### Features

- HVCMOS® technology
- Output voltages up to 180V
- Low power level shifting
- Shift register speed: 6MHz @  $V_{DD} = 5V$   
12MHz @  $V_{DD} = 12V$
- Latched data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

### General Description

The HV34 is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a printer driver for inkjet applications. It can also be used in any application requiring multiple output high voltage, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded,  $D_{IOA}$  is Data-In and  $D_{IOB}$  is Data-Out; data is shifted from  $HV_{OUT64}$  to  $HV_{OUT1}$ . When DIR is at logic high,  $D_{IOB}$  is Data-In and  $D_{IOA}$  is Data-Out; data is then shifted from  $HV_{OUT1}$  to  $HV_{OUT64}$ . Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the  $\overline{LE}$  (latch enable),  $\overline{BL}$  (blinking), or the  $\overline{POL}$  (polarity) inputs. Transfer of data from the shift register to the latch occurs when the  $\overline{LE}$  (latch enable) is high. The data in the latch is stored during  $\overline{LE}$  transition from high to low.

### Absolute Maximum Ratings<sup>1</sup>

Supply voltage, $V_{DD}$	-0.5V to +15V	
Supply voltage, $V_{PP}$	$V_{DD}$ to +200V	
Logic input levels	-0.5V to $V_{DD} + 0.5V$	
Ground current <sup>2</sup>	1.5A	
High voltage supply current <sup>2</sup>	1.3A	
Continuous total power dissipation <sup>3</sup>	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Ceramic	-55°C to +125°C
	Plastic	-40°C to +85°C
Storage temperature range	-65°C to +150°C	

#### Notes:

1. All voltages are referenced to GND.
2. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 31.7mW/°C for ceramic.

# Electrical Characteristics (over recommended operating conditions unless noted)

## DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{DD}$	$V_{DD}$ Supply Current			25	mA	$f_{CLK} = 12\text{MHz}$ , $f_{DATA} = 12\text{MHz}$ $\overline{LE} = \text{LOW}$
$I_{DDQ}$	Quiescent $V_{DD}$ Supply Current			200	$\mu\text{A}$	All $V_{IN} = 0\text{V}$ or $V_{DD}$
$I_{PP}$	High Voltage Supply Current			0.50	mA	$V_{PP} = 180\text{V}$ All outputs high
				0.50	mA	$V_{PP} = 180\text{V}$ All outputs low
$I_{IH}$	High-Level Logic Input Current			10	$\mu\text{A}$	$V_{IH} = V_{DD}$
$I_{IL}$	Low-Level Logic Input Current			-10	$\mu\text{A}$	$V_{IL} = 0\text{V}$
$V_{OH}$	High-Level Output	HV <sub>OUT</sub>	155		V	$V_{PP} = 180\text{V}$ , IHV <sub>OUT</sub> = -5mA ID <sub>OUT</sub> = -100 $\mu\text{A}$
		Data Out	$V_{DD} - 1\text{V}$		V	
$V_{OL}$	Low-Level Output	HV <sub>OUT</sub>		25	V	$V_{PP} = 180\text{V}$ , IHV <sub>OUT</sub> = +5mA ID <sub>OUT</sub> = +100 $\mu\text{A}$
		Data Out		1.0	V	
$V_{OC}$	HV <sub>OUT</sub> Clamp Voltage			$V_{PP} + 1.5$	V	$I_{OL} = +5\text{mA}$
				-1.5	V	$I_{OL} = -5\text{mA}$

## AC Characteristics<sup>1,2</sup> (For $V_{DD} = 12\text{V}$ : values in parentheses are for $V_{DD} = 5\text{V}$ ; $V_{PP} = 180\text{V}$ , $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$f_{CLK}$	Clock Frequency			12(6)	MHz	
$t_W$	Clock Width High and Low				ns	High
$t_{SU}$	Data Setup Time Before Clock Rises	25(35)			ns	
$t_H$	Data Hold Time After Clock Rises	10(30)			ns	
$t_{WLE}$	Width of Latch Enable Pulse	62(80)			ns	
$t_{DLE}$	$\overline{LE}$ Delay Time Rising Edge of Clock	25(35)			ns	
$t_{SLE}$	$\overline{LE}$ Setup Time Before Rising Edge of Clock	30(40)			ns	
$t_{ON}, t_{OFF}$	Time from Latch Enable to HV <sub>OUT</sub>			1(1.5)	$\mu\text{s}$	$C_L = 20\text{pF}$
$t_{DHL}$	Delay Time Clock to Data High to Low			50(110)	ns	$C_L = 20\text{pF}$
$t_{DLH}$	Delay Time Clock to Data Low to High			75(160)	ns	$C_L = 20\text{pF}$
$t_r, t_f$	All Logic Inputs			5	ns	

### Notes:

- Shift register speed can be as low as DC as long as Data Set-up and Hold Time meet the spec.
- AC Characteristics are guaranteed only under  $V_{DD} = 12\text{V}$  and  $V_{DD} = 5\text{V}$ .

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	
$V_{DD}$	Logic supply voltage	$V_{DD} = 5\text{V}$	4.5	5.0	5.5	V
		$V_{DD} = 12\text{V}$	10.8	12.0	13.2	V
$V_{PP}$	High voltage supply	60		180	V	
$V_{IH}$	High-level input voltage	$V_{DD} - 0.9$		$V_{DD}$	V	
$V_{IL}$	Low-level input voltage	0		0.9	V	
$T_A$	Operating free-air temperature	Plastic	-40		+85	$^\circ\text{C}$
		Ceramic	-55		+125	

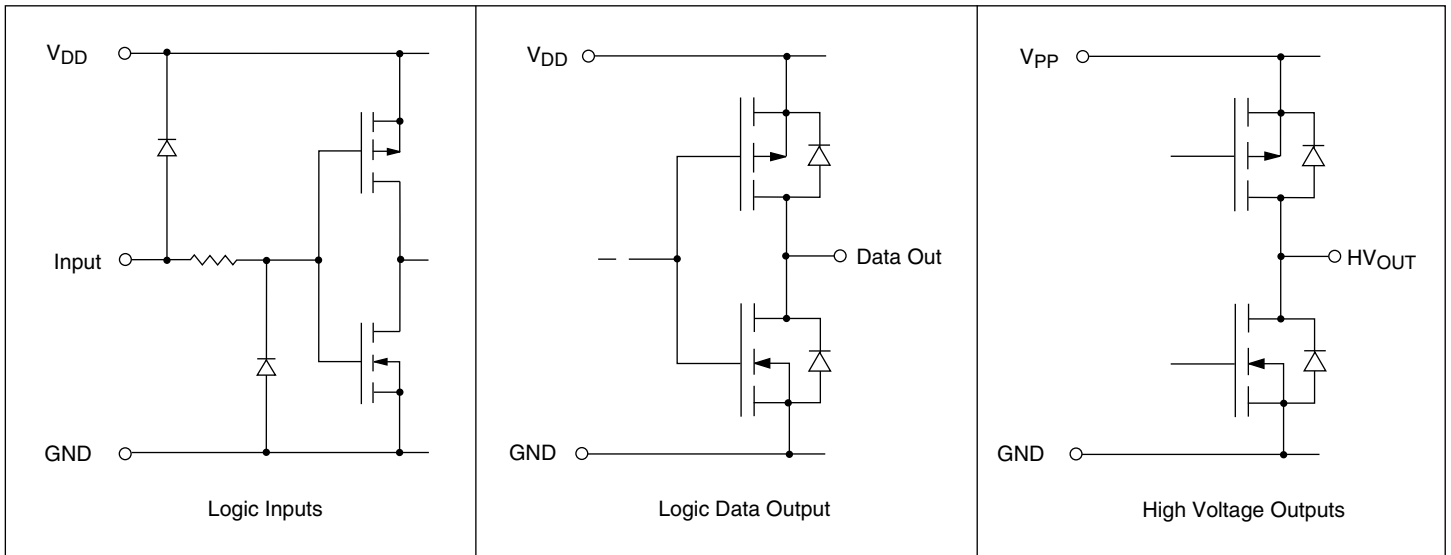
### Notes:

Power-up sequence should be the following:

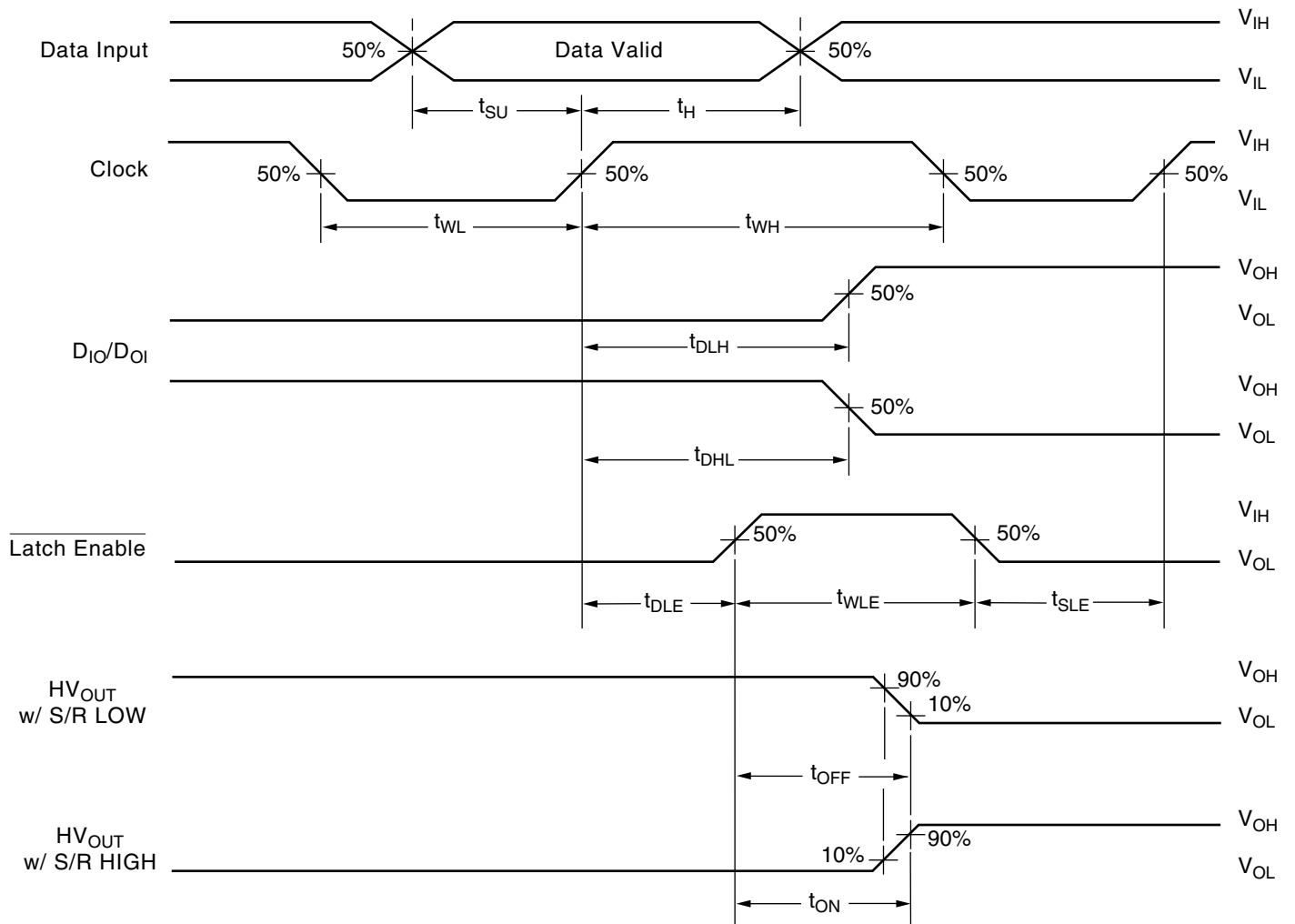
- Connect ground.
- Apply  $V_{DD}$ .
- Set all inputs (Data, CLK, Enable, etc.) to a known state.
- Apply  $V_{PP}$ .
- The  $V_{PP}$  should not drop below  $V_{DD}$  or float during operation.

Power-down sequence should be the reverse of the above.

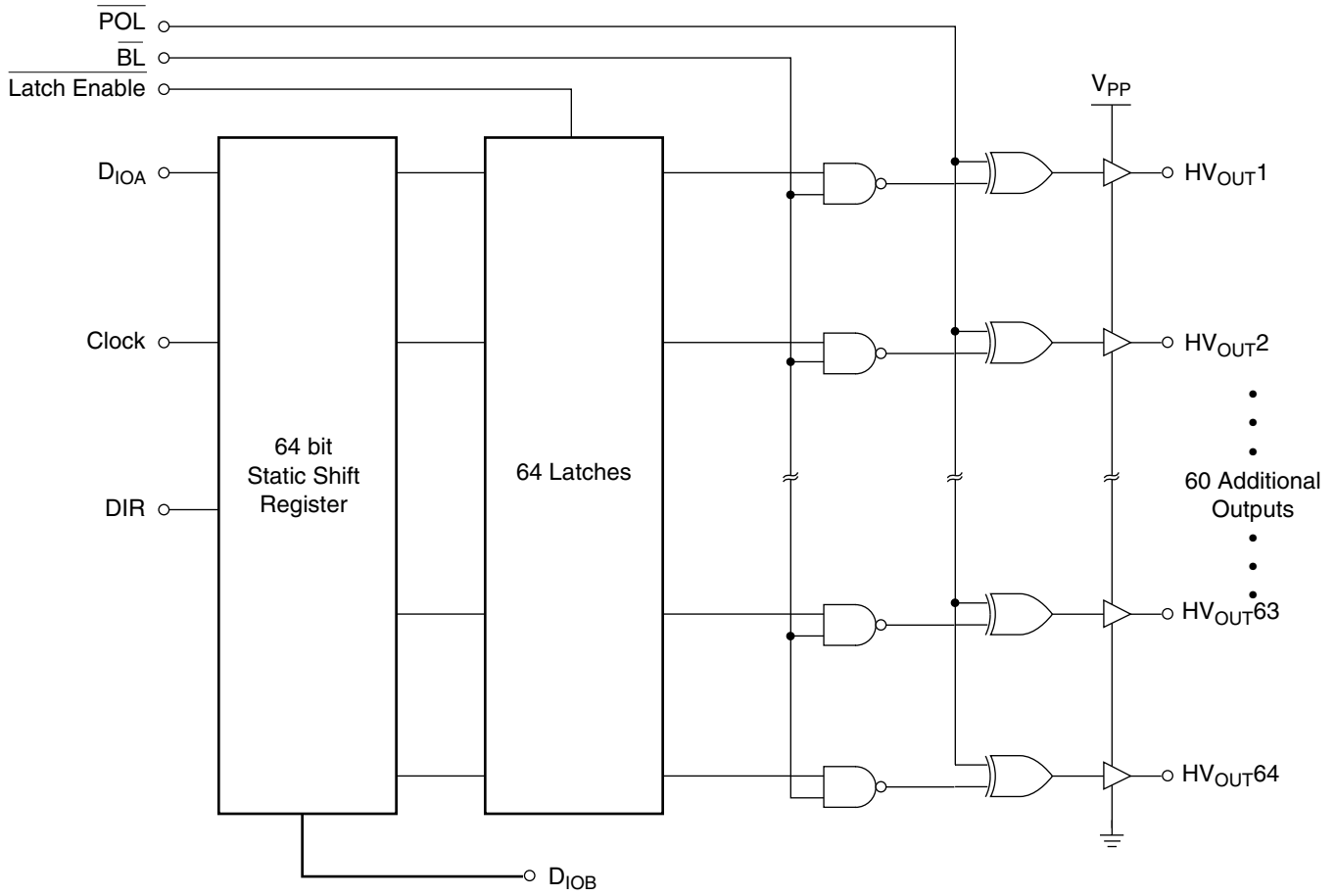
# Input and Output Equivalent Circuits



# Switching Waveforms



# Functional Block Diagram



# Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg 1 2...64	HV Outputs 1 2...64		Data Out *	
All on	X	X	X	L	L	X	* *...*	H H...H		*	
All off	X	X	X	L	H	X	* *...*	L L...L		*	
Invert mode	X	X	L	H	L	X	* *...*	$\overline{*}$ $\overline{*}$ ...		*	
Load S/R	H or L	↑	L	H	H	X	H or L *...*	* *...*		*	
Load/Store Data in Latches	X	X	↓	H	H	X	* *...*	* *...*		*	
	X	X	↓	H	L	X	* *...*	$\overline{*}$ $\overline{*}$ ...		*	
Transparent Latch mode	L	↑	H	H	H	X	L *...*	L *...*		*	
	H	↑	H	H	H	X	H *...*	H *...*		*	
I/O Relation	D <sub>IOA</sub>	↑	X	X	X	L	Q <sub>n</sub> → Q <sub>n-1</sub>	—		D <sub>IOB</sub>	
	D <sub>IOB</sub>	↑	X	X	X	H	Q <sub>n</sub> → Q <sub>n+1</sub>	—		D <sub>IOA</sub>	

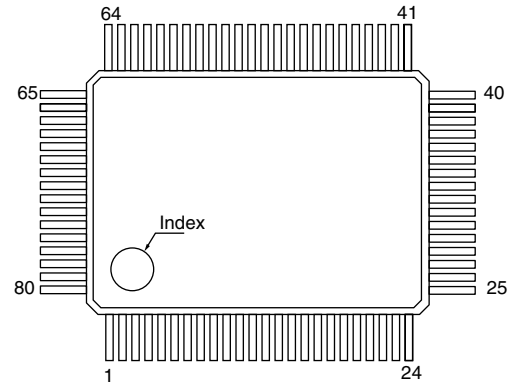
**Notes:**  
 H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.  
 \* = dependent on previous stage's state before the last CLK or last  $\overline{LE}$  high.

## Pin Configurations

### HV34

Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 41/24	41	HV <sub>OUT</sub> 1/64
2	HV <sub>OUT</sub> 42/23	42	HV <sub>OUT</sub> 2/63
3	HV <sub>OUT</sub> 43/22	43	HV <sub>OUT</sub> 3/62
4	HV <sub>OUT</sub> 44/21	44	HV <sub>OUT</sub> 4/61
5	HV <sub>OUT</sub> 45/20	45	HV <sub>OUT</sub> 5/60
6	HV <sub>OUT</sub> 46/19	46	HV <sub>OUT</sub> 6/59
7	HV <sub>OUT</sub> 47/18	47	HV <sub>OUT</sub> 7/58
8	HV <sub>OUT</sub> 48/17	48	HV <sub>OUT</sub> 8/57
9	HV <sub>OUT</sub> 49/16	49	HV <sub>OUT</sub> 9/56
10	HV <sub>OUT</sub> 50/15	50	HV <sub>OUT</sub> 10/55
11	HV <sub>OUT</sub> 51/14	51	HV <sub>OUT</sub> 11/54
12	HV <sub>OUT</sub> 52/13	52	HV <sub>OUT</sub> 12/53
13	HV <sub>OUT</sub> 53/12	53	HV <sub>OUT</sub> 13/52
14	HV <sub>OUT</sub> 54/11	54	HV <sub>OUT</sub> 14/51
15	HV <sub>OUT</sub> 55/10	55	HV <sub>OUT</sub> 15/50
16	HV <sub>OUT</sub> 56/9	56	HV <sub>OUT</sub> 16/49
17	HV <sub>OUT</sub> 57/8	57	HV <sub>OUT</sub> 17/48
18	HV <sub>OUT</sub> 58/7	58	HV <sub>OUT</sub> 18/47
19	HV <sub>OUT</sub> 59/6	59	HV <sub>OUT</sub> 19/46
20	HV <sub>OUT</sub> 60/5	60	HV <sub>OUT</sub> 20/45
21	HV <sub>OUT</sub> 61/4	61	HV <sub>OUT</sub> 21/44
22	HV <sub>OUT</sub> 62/3	62	HV <sub>OUT</sub> 22/43
23	HV <sub>OUT</sub> 63/2	63	HV <sub>OUT</sub> 23/42
24	HV <sub>OUT</sub> 64/1	64	HV <sub>OUT</sub> 24/41
25	V <sub>PP</sub>	65	HV <sub>OUT</sub> 25/40
26	D <sub>IOA</sub>	66	HV <sub>OUT</sub> 26/39
27	N/C	67	HV <sub>OUT</sub> 27/38
28	N/C	68	HV <sub>OUT</sub> 28/37
29	$\overline{\text{BL}}$	69	HV <sub>OUT</sub> 29/36
30	$\overline{\text{POL}}$	70	HV <sub>OUT</sub> 30/35
31	V <sub>DD</sub>	71	HV <sub>OUT</sub> 31/34
32	DIR	72	HV <sub>OUT</sub> 32/33
33	LGND	73	HV <sub>OUT</sub> 33/32
34	OGND	74	HV <sub>OUT</sub> 34/31
35	N/C	75	HV <sub>OUT</sub> 35/30
36	N/C	76	HV <sub>OUT</sub> 36/29
37	CLK	77	HV <sub>OUT</sub> 37/28
38	$\overline{\text{LE}}$	78	HV <sub>OUT</sub> 38/27
39	D <sub>IOB</sub>	79	HV <sub>OUT</sub> 39/26
40	V <sub>PP</sub>	80	HV <sub>OUT</sub> 40/25

## Package Outline



top view

80-pin Gullwing Package

### Note:

Pin designation for DIR = H/L

Example: for DIR = H, Pin 1 is HV<sub>OUT</sub>41  
for DIR = L, Pin 1 is HV<sub>OUT</sub>24