

High Voltage Liquid Crystal Shutter Driver

Ordering Information

Device	HV _{IN} Maximum Voltage	Package Options
		SO-8
HV508	45V	HV508LG

Features

- ❑ HVCMOS® technology for high performance
- ❑ Logic-selectable output voltage
- ❑ 100nF drive capability
- ❑ Up to 90V_{P-P}
- ❑ 25µs response time

General Description

The Supertex HV508 is a 45V liquid crystal shutter driver in an SO-8 surface mount package. It consists of two outputs that provide square waves of opposite phase. The liquid crystal shutter is connected between the two outputs. Its equivalent load can be approximated as a resistor in parallel with a capacitor. Minimum resistance is 1.0MΩ and maximum capacitance is 0.1µF.

The HV508 has three input supply voltages, HV_{IN}, LV_{IN}, and V_{DD}. The output's amplitude will be either LV_{IN} or HV_{IN}. A logic high on the HV_{EN} input will set the output to operate from the HV_{IN} supply. A logic low on the HV_{EN} input will set the output to operate from the LV_{IN} supply. The output frequency is set by the logic input frequency applied on the POL input.

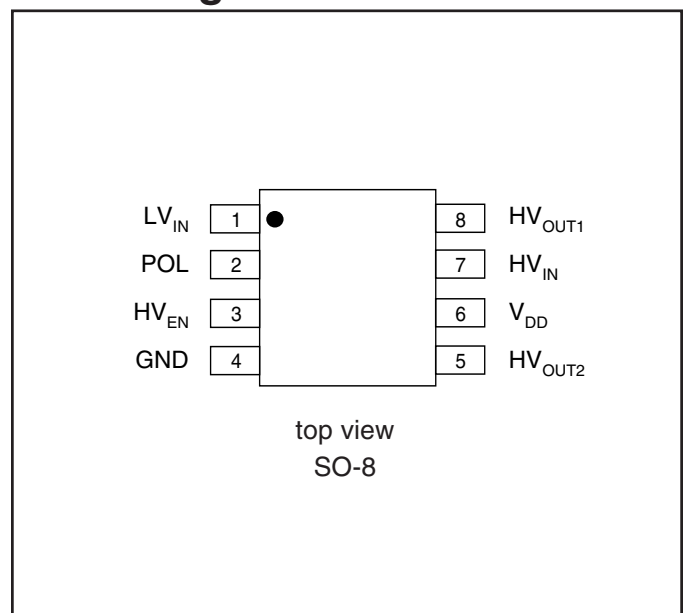
Absolute Maximum* Ratings

HV _{IN} , high voltage input	+60V
LV _{IN} , low voltage input	+7.5V
V _{DD} , logic supply voltage	+12V
Continuous total power dissipation	700mW
Operating temperature	-5°C to +60°C
Storage temperature	-65°C to +150°C
Soldering temperature	+300°C

* All voltages are referenced to GND.

For operation above 25°C ambient derate linearly at 6mW/°C.

Pin Configuration



Electrical Characteristics

DC Electrical Characteristics (over operating supply voltages unless otherwise specified, $T_A = -5^{\circ}\text{C}$ to $+60^{\circ}\text{C}$)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
I_{HVQ}	HV_{IN} quiescent current			10	μA	
I_{LVQ}	LV_{IN} quiescent current			10	μA	
I_{DDQ}	V_{DD} quiescent current			10	μA	
I_{HV}	HV_{IN} operating current			2.8	mA	POL = 100Hz, HV_{EN} = high, $T_A = 25^{\circ}\text{C}$, Load = $1\text{M}\Omega$ in parallel with $0.1\mu\text{F}$ between HV_{OUT1} and HV_{OUT2}
I_{LV}	LV_{IN} operating current			380	μA	POL = 100Hz, HV_{EN} = low, $T_A = 25^{\circ}\text{C}$, Load = $1\text{M}\Omega$ in parallel with $0.1\mu\text{F}$ between HV_{OUT1} and HV_{OUT2}
I_{IL}	Logic input current low	-5			μA	
I_{IH}	Logic input current high			5.0	μA	
C_{LOAD}	Output capacitive load*	0		0.25	μF	C_{LOAD} in parallel with a $1\text{M}\Omega$ resistor

*The device can operate continuously without any damage within this range. AC limits are not implemented.

AC Electrical Characteristics ($HV_{IN} = 45\text{V}$, $LV_{IN} = 6\text{V}$, $V_{DD} = 5\text{V}$, $T_A = -5^{\circ}\text{C}$ to $+60^{\circ}\text{C}$)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
f_{POL}	POL input frequency	0		100	Hz	
$t_{HV(ON)}$	Turn-on time when high voltage is enable			16	μs	Load = $1\text{M}\Omega$ in parallel with $0.1\mu\text{F}$ between HV_{OUT1} and HV_{OUT2} . HV_{EN} = High. Outputs rise to HV_{IN} . See Fig. 1.
$t_{HV(OFF)}$	Turn-off time when high voltage is enabled			16	μs	
$t_{LV(ON)}$	Turn-on time when high voltage is disabled			40	μs	Load = $1\text{M}\Omega$ in parallel with $0.1\mu\text{F}$ between HV_{OUT1} and HV_{OUT2} . HV_{EN} = Low. Outputs rise to LV_{IN} . See Fig. 1.
$t_{LV(OFF)}$	Turn-off time when high voltage is disabled			6.0	μs	
$t_{EN(ON)}$	Turn-on time from HV_{EN} to HV_{OUT}			25	μs	Load = $1\text{M}\Omega$ in parallel with $0.1\mu\text{F}$ between HV_{OUT1} and HV_{OUT2} . See Fig. 2.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Logic supply voltage	5.0		10.0	V
LV_{IN}	Low output supply voltage	3.0		6.0	V
HV_{IN}	High output supply voltage	5.0		45	V
V_{IL}	Logic input voltage low	0		$0.3V_{DD}$	V
V_{IH}	Logic input voltage high	$0.7V_{DD}$		V_{DD}	V
T_A	Ambient Temperature	-5.0		+60	$^{\circ}\text{C}$

Notes:

Power-up sequence should be the following:

1. Connect GND, V_{DD} , logic inputs, HV_{IN} , and LV_{IN} .

Power-down sequence should be the reverse of the above.

Truth Table

HV _{EN}	POL	HV _{OUT1}	HV _{OUT2}
H	H	HV _{IN}	GND
H	L	GND	HV _{IN}
L	H	LV _{IN}	GND
L	L	GND	LV _{IN}

Timing Diagram

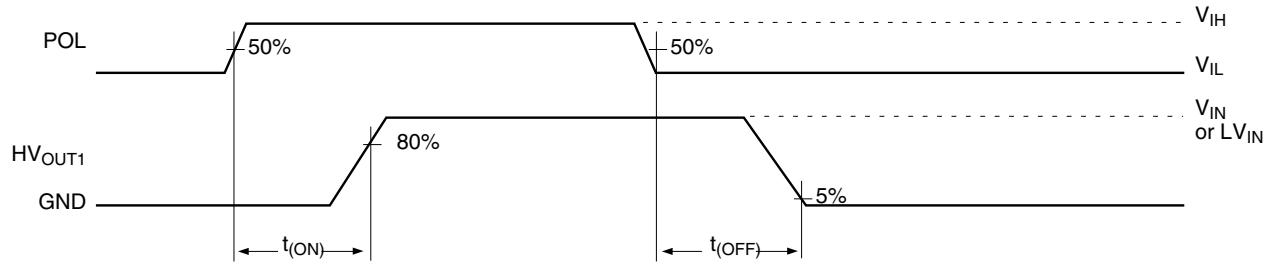


Figure 1

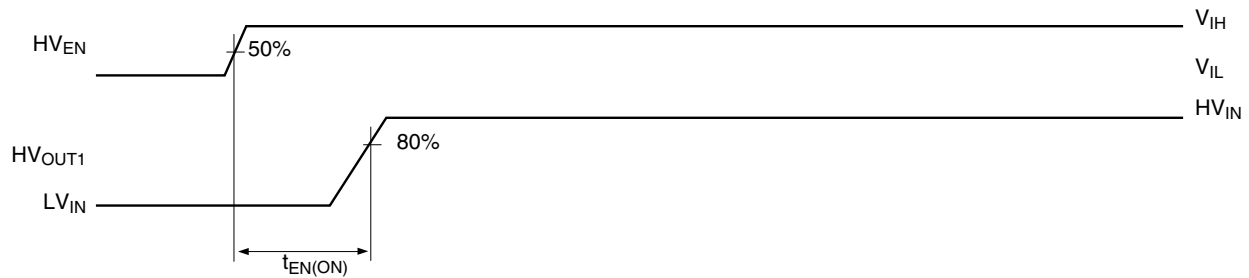


Figure 2

Block Diagram

