

## 40MHz, 32-Channel Serial to Parallel Converter with Push-Pull Outputs

### Ordering Information

Device	Package Options		
	64 Pin Plastic Gullwing	80-Lead Ceramic Gullwing	Die in Wafer Form
HV76	HV7620PG	HV7620DG	HV7620XW

### Features

- Processed with HVCMOS® technology
- 5V CMOS logic and 12V supply rail
- Output voltage up to 200V
- Low power level shifting
- Source/sink current minimum 50mA
- 40MHz equivalent data rate
- Chip select
- Polarity function
- Forward and reverse shifting options (DIR pin)
- Latched outputs

### General Description

The HV76 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

The device has 4 parallel 8-bit shift registers permitting data rate 4 times the speed of one. The data are clocked in simultaneously on all four data inputs with a single clock. Data are shifted in on a low to high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to  $V_{DD1}$ , and counterclockwise (CCW) shifting when connected to GND. Operation of the shift register is not affected by the  $\overline{LE}$  (latch enable) input. Transfer of data from the shift registers to the latches occurs when the  $\overline{LE}$  input is high. Data is stored in the latches when  $\overline{LE}$  is low. The current source on the logic inputs provides active pull up when the input pins are open.

### Absolute Maximum Ratings

Supply voltage <sup>1</sup> , $V_{DD1}$		-0.5V to +15V
Supply voltage <sup>1</sup> , $V_{DD2}$		-0.5V to +15V
Supply voltage <sup>1</sup> , $V_{PP}$		-0.5V to +225V
Logic input levels <sup>1</sup>		-2.0V to $V_{DD1}+2.0V$
Continuous total power dissipation <sup>2</sup>	Plastic	1200mW
	Ceramic	1900mW
Operating temperature range	Plastic	-40°C to +85°C
	Ceramic	-55°C to 125°C
Storage temperature range		-65°C to +150°C

#### Notes:

1. All voltages are referenced to GND.
2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 19mW/°C for ceramic.

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## Electrical Characteristics (over recommended operating conditions unless noted)

### DC Characteristics ( $V_{DD1} = 5V$ , $V_{DD2} = 12V$ , $V_{PP} = 200V$ and $T_A = 25^\circ C$ )

Symbol	Parameters	Min	Max	Units	Condition
$I_{DD1}$	$V_{DD1}$ supply current		5	mA	$f_{CLK} = 10MHz$
$I_{DD2}$	$V_{DD2}$ supply current		20	mA	$V_{DD2} = V_{DD2} \text{ max}$ $f_{CLK} = 10 \text{ MHz}$
$I_{PP}$	High voltage supply current		2	mA	All output high or low
$I_{DD1Q}$	Quiescent $V_{DD1}$ supply current		100	$\mu A$	All input = $V_{DD1}$
$I_{DD2Q}$	Quiescent $V_{DD2}$ supply current		100	$\mu A$	All input = $V_{DD1}$
$V_{OH}$	High-level output	185		V	$I_O = -50mA$
$V_{OL}$	Low-level output		20	V	$I_O = 50mA$
$I_{IH}$	High-level logic input current		1.0	$\mu A$	$V_{IN} = V_{DD1}$
$I_{IL}$	Low-level logic input current		-10	$\mu A$	$V_{IN} = 0V$
$V_{GG}$	HVGND to LVGND voltage difference	-1.0	1.0	V	

### AC Characteristics (Logic signal inputs and data inputs have $t_r, t_f \leq 5ns$ . $V_{DD1} = 5V$ or $12V$ , $V_{DD2} = 12V$ , $V_{PP} = 200V$ )

Symbol	Parameters	Min	Max	Units	Condition
$f_{CLK}$	Clock frequency	$V_{DD1} = 5V$	10	MHz	Per register $C_L = 15pF$
		$V_{DD1} = 12V$	5	MHz	Per register $C_L = 15pF$
$t_{WL}, t_{WH}$	Clock width high or low	40		ns	
$t_{SU}$	Data set-up time	20		ns	
$t_H$	Data hold time	20		ns	
$t_{ON}, t_{OFF}$	Time from $\overline{LE}$ to $HV_{OUT}$		275	ns	$C_L = 15pF$
$t_{WLE}$	Width of $\overline{LE}$ pulse	25		ns	
$t_{DLE}$	Delay time clock to $\overline{LE}$ low to high	50		ns	
$t_{SLE}$	$\overline{LE}$ setup time before clock rises	20		ns	
$t_{DLF}, t_{DLN}$	$\overline{BL}$ or $\overline{CS}$ low to high to $HV_{OUT}$		250	ns	
$t_{COF}, t_{CON}$	Clock to $HV_{OUT}$		275	ns	
$t_{DLH}$	Delay time clock to data low to high		100	ns	$C_L = 15pF$
$t_{DHL}$	Delay time clock to data high to low		100	ns	$C_L = 15pF$

## Recommended Operating Conditions

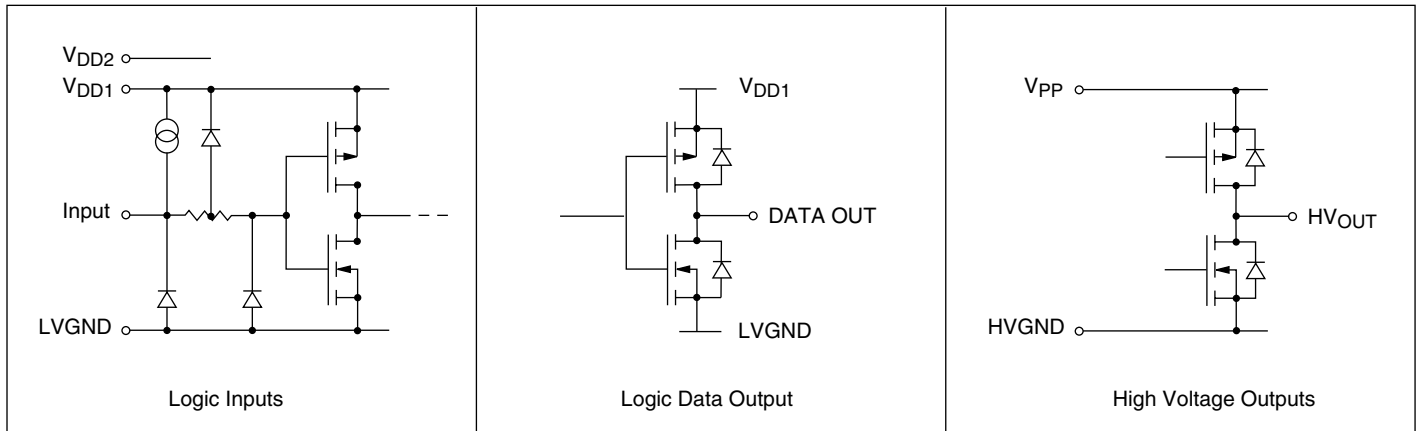
Symbol	Parameters	Min	Max	Unit	
$V_{DD1}$	Logic supply voltage	4.5	$V_{DD2}$	V	
$V_{DD2}$	12V supply voltage	10.8	13.2	V	
$V_{PP}$	High voltage supply voltage	50	200	V	
$V_{IH}$	High-level input voltage	$V_{DD1} - 0.5V$	$V_{DD1}$	V	
$V_{IL}$	Low-level input voltage	0	0.5	V	
$f_{CLK}$	Clock frequency	$V_{DD1} = 5V$	10	MHz	
		$V_{DD1} = 12V$	5	MHz	
$T_A$	Operating free-air temperature	Plastic	-40	+85	$^\circ C$
		Ceramic	-55	+125	$^\circ C$
$I_{OD}$	Allowable pulsed current through output diodes <sup>1</sup>		500	mA	
$I_{GND(VPP)}$	Allowable pulsed $V_{PP}$ or HVGND current <sup>1</sup>		16	A	
$V_{PP(SLEW)}^2$	Slew rate of $V_{PP}$		340	V/ $\mu s$	

#### Notes:

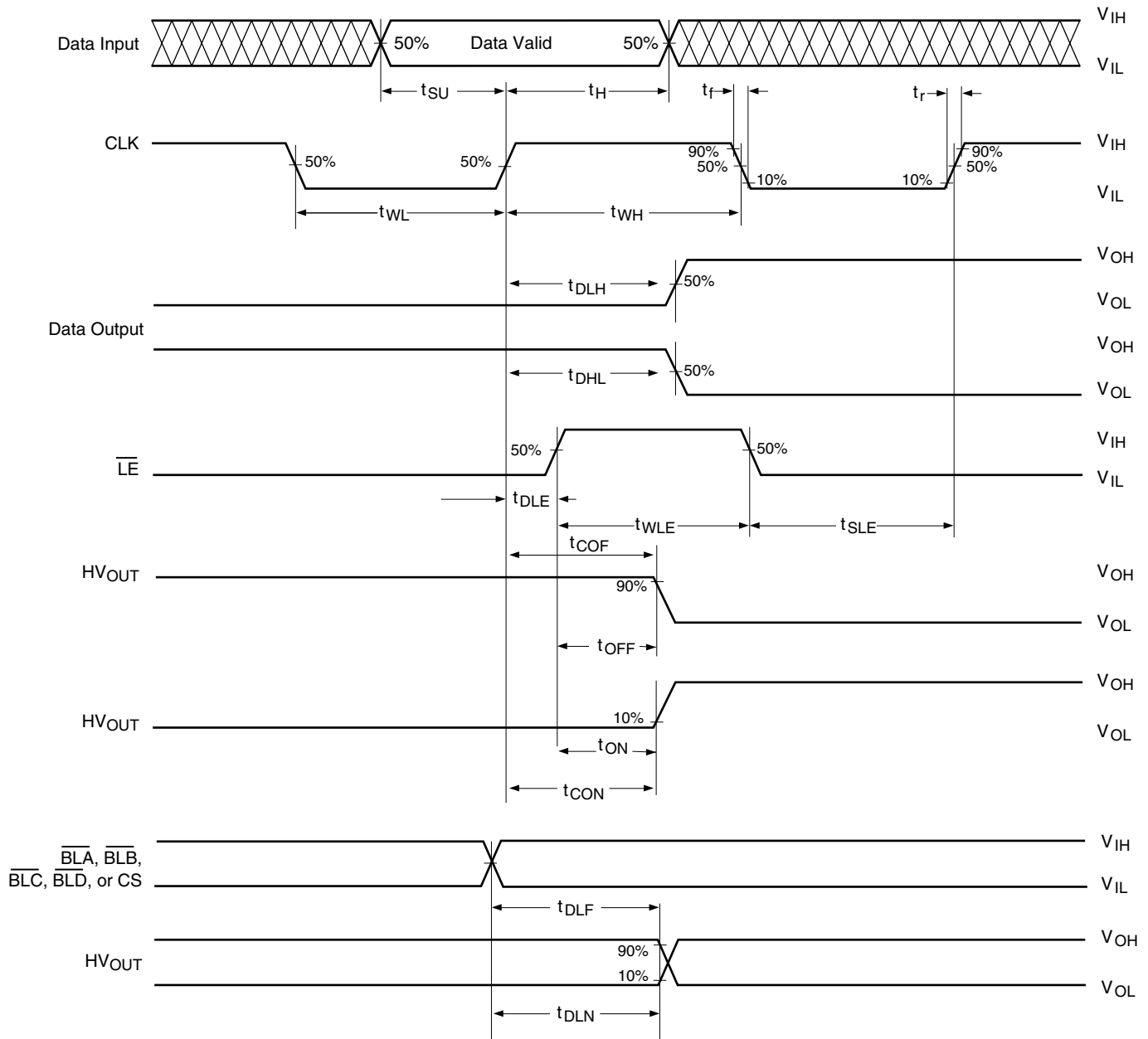
1.The current pulse width = 500ns, duty cycle = 5%.

2.This device cannot be hot-switched for output frequency greater than 500Hz. For output frequency greater than 500Hz,  $V_{PP}$  must be ramped.

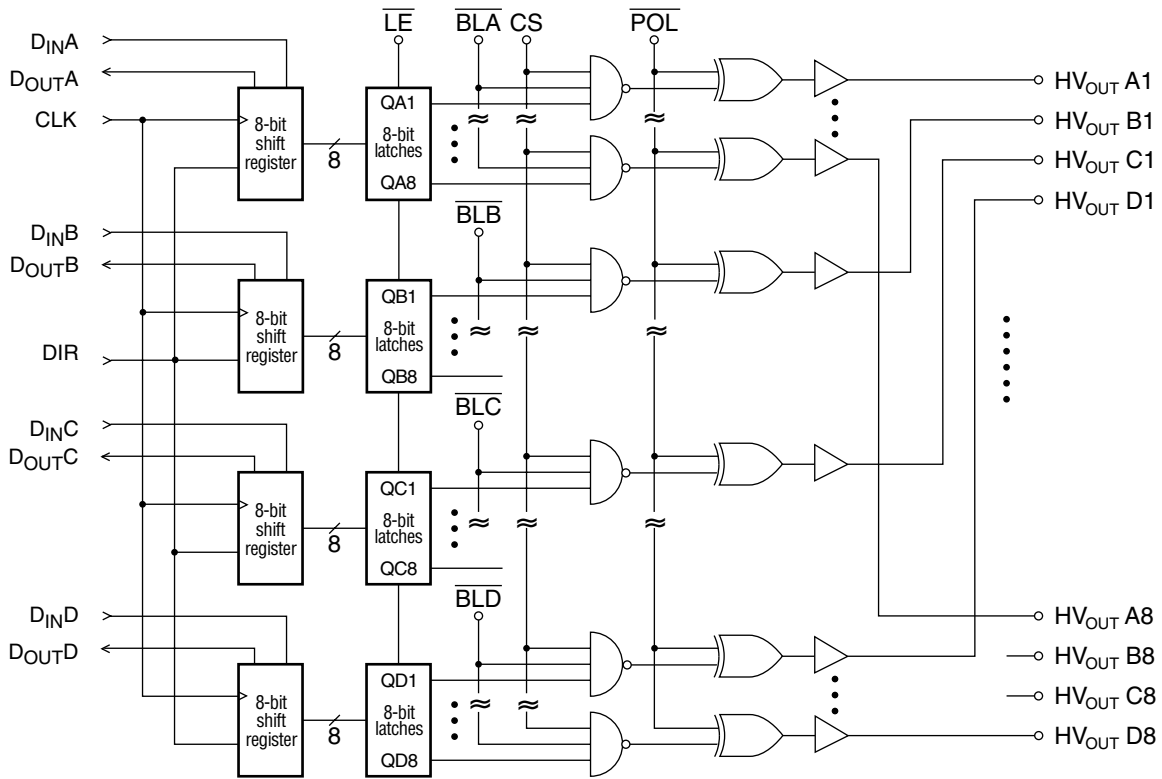
# Input and Output Equivalent Circuits



# Switching Waveforms



# Functional Block Diagram



# Function Table

Function	Inputs													HV Outputs				
	D <sub>INA</sub>	D <sub>INB</sub>	D <sub>INC</sub>	D <sub>IND</sub>	CLK	LE	DIR	BLA	BLB	BLC	BLD	CS	POL	A	B	C	D	
All O/P High	X	X	X	X	X	X	X	X	X	X	X	X	L	L	H	H	H	H
All O/P Low	X	X	X	X	X	X	X	X	X	X	X	X	L	H	L	L	L	L
"A" Outputs Low	X	X	X	X	X	X	X	L	X	X	X	X	H	L	*	*	*	*
Normal Polarity	X	X	X	X	X	X	X	H	H	H	H	H	H	No Inversion				
Outputs Inverted	X	X	X	X	X	X	X	H	H	H	H	H	L	Inversion				
Transparent Mode	H	L	L	L	↑	H	X	H	H	H	H	H	H	H	L	L	L	L
Data Stored	X	X	X	X	X	L	X	H	H	H	H	H	H	Stored Data				
Shift CW	X	X	X	X	↑	H	H	H	H	H	H	H	X	A <sub>N</sub>	B <sub>N</sub>	C <sub>N</sub>	D <sub>N</sub>	
Shift CCW	X	X	X	X	↑	H	L	H	H	H	H	H	X	A <sub>N-1</sub>	B <sub>N-1</sub>	C <sub>N-1</sub>	D <sub>N-1</sub>	

**Notes:**

H = High level, L = Low level, X = Irrelevant, ↑ = Low to high transition.  
 \* = Dependent on previous stage's state before the last CLK ↑ for last LE high.

Power-up sequence:

- GND (HV, LV)
- V<sub>DD2</sub>
- V<sub>DD1</sub>
- Logic Input Signals
- V<sub>PP</sub>

To power down reverse the sequence above.

The V<sub>PP</sub> should not drop below V<sub>DD</sub> or float during operation.

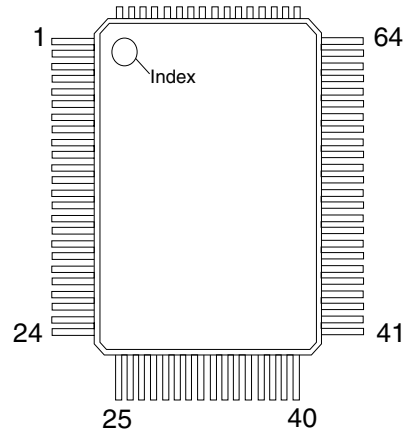
# Pin Configurations

## HV76

Pin	Function	Pin	Function
1	HVGND	33	CS
2	V <sub>PP</sub>	34	D <sub>OUT</sub> B
3	HV <sub>OUT</sub> D8	35	D <sub>IN</sub> B
4	HV <sub>OUT</sub> C8	36	D <sub>IN</sub> A
5	HV <sub>OUT</sub> B8	37	D <sub>OUT</sub> A
6	HV <sub>OUT</sub> A8	38	CLK
7	HV <sub>OUT</sub> D7	39	BLA
8	HV <sub>OUT</sub> C7	40	BLB
9	HV <sub>OUT</sub> B7	41	V <sub>DD1</sub>
10	HV <sub>OUT</sub> A7	42	LVGND
11	HV <sub>OUT</sub> D6	43	N/C
12	HV <sub>OUT</sub> C6	44	HVGND
13	HV <sub>OUT</sub> B6	45	HVGND
14	HV <sub>OUT</sub> A6	46	V <sub>PP</sub>
15	HV <sub>OUT</sub> D5	47	HV <sub>OUT</sub> D4
16	HV <sub>OUT</sub> C5	48	HV <sub>OUT</sub> C4
17	HV <sub>OUT</sub> B5	49	HV <sub>OUT</sub> B4
18	HV <sub>OUT</sub> A5	50	HV <sub>OUT</sub> A4
19	V <sub>PP</sub>	51	HV <sub>OUT</sub> D3
20	HVGND	52	HV <sub>OUT</sub> C3
21	HVGND	53	HV <sub>OUT</sub> B3
22	V <sub>DD2</sub>	54	HV <sub>OUT</sub> A3
23	BLC	55	HV <sub>OUT</sub> D2
24	BLD	56	HV <sub>OUT</sub> C2
25	LE	57	HV <sub>OUT</sub> B2
26	D <sub>OUT</sub> D	58	HV <sub>OUT</sub> A2
27	D <sub>IN</sub> D	59	HV <sub>OUT</sub> D1
28	D <sub>IN</sub> C	60	HV <sub>OUT</sub> C1
29	D <sub>OUT</sub> C	61	HV <sub>OUT</sub> B1
30	POL	62	HV <sub>OUT</sub> A1
31	LVGND	63	V <sub>PP</sub>
32	DIR	64	HVGND

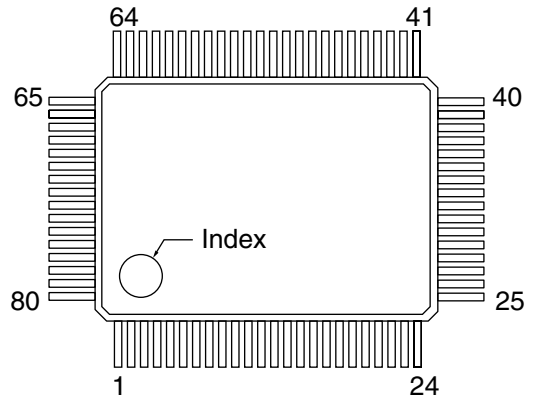
\*Pins 65 to 80 are N/C (ceramic only)

# Package Outline



top view

3-sided Plastic 64-pin Gullwing Package



top view

80-pin Ceramic Gullwing Package