



**N-Channel Enhancement-Mode
Vertical DMOS FETs**

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	V _{GS(th)} (max)	Order Number / Package
				Die*
60V	3.0Ω	2A	2.0V	TN1506NW
100V	3.0Ω	2A	2.0V	TN1510NW

* Die in wafer form.

Features

- Low threshold — 2.0V max.
- High input impedance
- Low input capacitance — 50pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C

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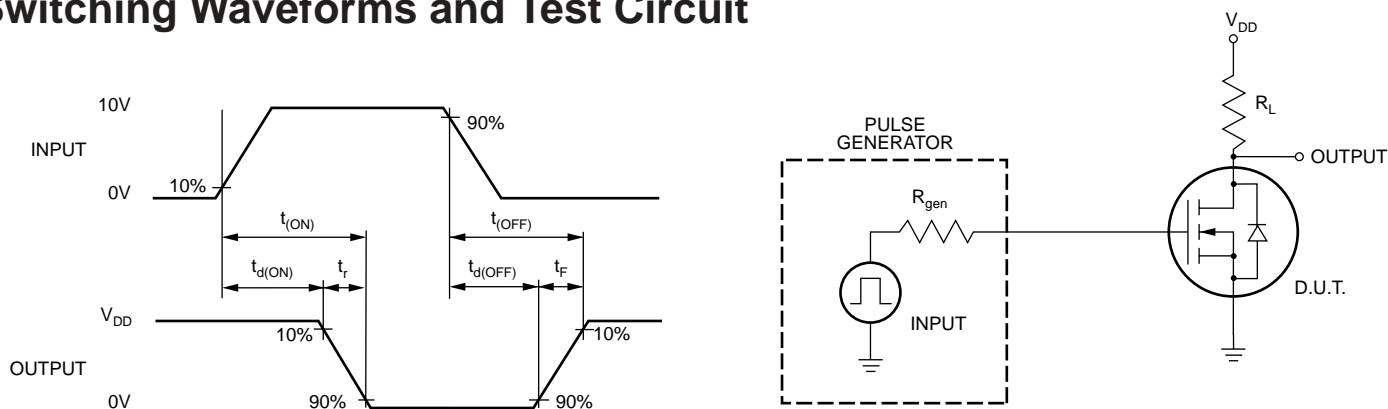
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	TN1510	100		V	I _D = 1mA, V _{GS} = 0V
		TN1506	60			
V _{GS(th)}	Gate Threshold Voltage	0.6		2.0	V	V _{GS} = V _{DS} , I _D = 0.5mA
ΔV _{GS(th)}	Change in V _{GS(th)} with Temperature		-3.2	-5.0	mV/°C	V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate Body Leakage			100	nA	V _{GS} = ±20V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current			10	μA	V _{GS} = 0V, V _{DS} = Max Rating
				500		V _{GS} = 0V, V _{DS} = 0.8 Max Rating T _A = 125°C
I _{D(ON)}	ON-State Drain Current	0.75	1.4		A	V _{GS} = 5V, V _{DS} = 25V
		2.0	3.4			V _{GS} = 10V, V _{DS} = 25V
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance		2.0	4.5	Ω	V _{GS} = 4.5V, I _D = 250mA
			1.6	3.0		V _{GS} = 10V, I _D = 500mA
ΔR _{DS(ON)}	Change in R _{DS(ON)} with Temperature		0.6	1.1	%/°C	I _D = 0.5A, V _{GS} = 10V
G _{FS}	Forward Transconductance	225	400		mS	V _{DS} = 25V, I _D = 500mA
C _{ISS}	Input Capacitance		50	60	pF	V _{GS} = 0V, V _{DS} = 25V f = 1 MHz
C _{OSS}	Common Source Output Capacitance		25	35		
C _{RSS}	Reverse Transfer Capacitance		4.0	8.0		
t _{d(ON)}	Turn-ON Delay Time		2.0	5.0	ns	V _{DD} = 25V I _D = 1.0A R _{GEN} = 25Ω
t _r	Rise Time		3.0	5.0		
t _{d(OFF)}	Turn-OFF Delay Time		6.0	7.0		
t _f	Fall Time		3.0	6.0		
V _{SD}	Diode Forward Voltage Drop		1.0	1.5	V	I _{SD} = 0.5A, V _{GS} = 0V
t _{rr}	Reverse Recovery Time		400		ns	I _{SD} = 0.5A, V _{GS} = 0V

Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



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