



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	V _{GS(th)} (max)	Order Number / Package	
			TO-243AA**	TO-236AB*
240V	15Ω	2.0V	TN2124N8	TN2124K1

Product marking for SOT-23: <div style="border: 1px solid black; padding: 2px; display: inline-block;">N1C*</div> where * = 2-week alpha date code
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* Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

** Product supplied on 2000 piece carrier tape reels.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{iss} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Advanced DMOS Technology

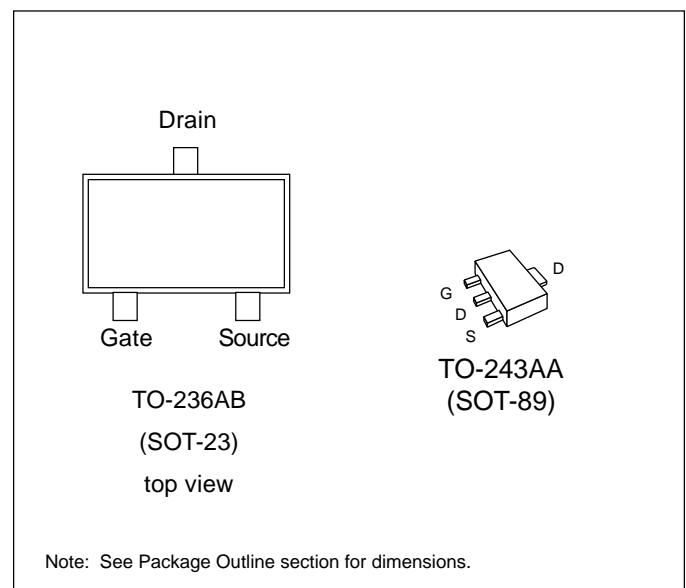
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-236AB	134mA	250mA	0.36W	200	350	134mA	250mA
TO-243AA	230mA	1.1A	1.6W†	15	78†	230mA	1.1A

* I_D (continuous) is limited by max rated T_j .

† Mounted on FR5 board. 25mmx25mmx1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

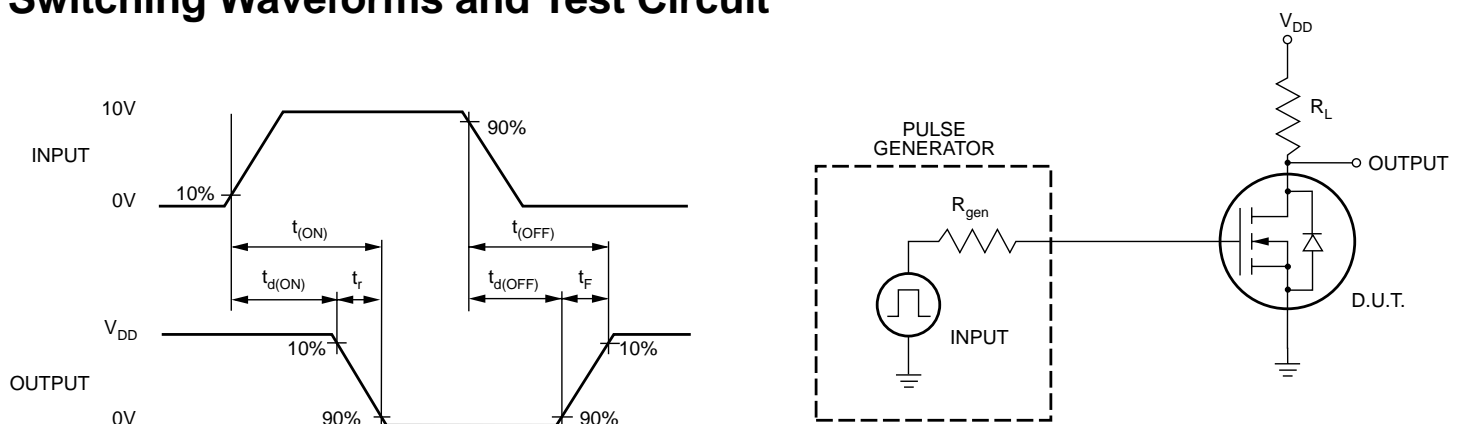
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	240			V	$I_D = 1\text{mA}$, $V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.5	mV/ $^\circ\text{C}$	$I_D = 1\text{mA}$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage		0.1	100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	$V_{GS} = 0\text{V}$, $V_{DS} = \text{Max Rating}$
				100	μA	$V_{GS} = 0\text{V}$, $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	140			mA	$V_{GS} = 4.5\text{V}$, $V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			30	Ω	$V_{GS} = 3\text{V}$, $I_D = 25\text{mA}$
				15	Ω	$V_{GS} = 4.5\text{V}$, $I_D = 120\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.7	1.0	%/ $^\circ\text{C}$	$I_D = 120\text{mA}$, $V_{GS} = 4.5\text{V}$
G_{FS}	Forward Transconductance	100	170		$\text{m}^{\overline{\Omega}}$	$V_{DS} = 25\text{V}$, $I_D = 120\text{mA}$
C_{ISS}	Input Capacitance		38	50	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$
C_{OSS}	Common Source Output Capacitance		9	15		
C_{RSS}	Reverse Transfer Capacitance		3	5		
$t_{d(ON)}$	Turn-ON Delay Time		4	7	ns	$V_{DD} = 25\text{V}$ $I_D = 140\text{mA}$ $R_{GEN} = 25\Omega$
t_r	Rise Time		2	5		
$t_{d(OFF)}$	Turn-OFF Delay Time		7	10		
t_f	Fall Time		9	12		
V_{SD}	Diode Forward Voltage Drop			1.8	V	$I_{SD} = 120\text{mA}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time		400		ns	$I_{SD} = 120\text{mA}$, $V_{GS} = 0\text{V}$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

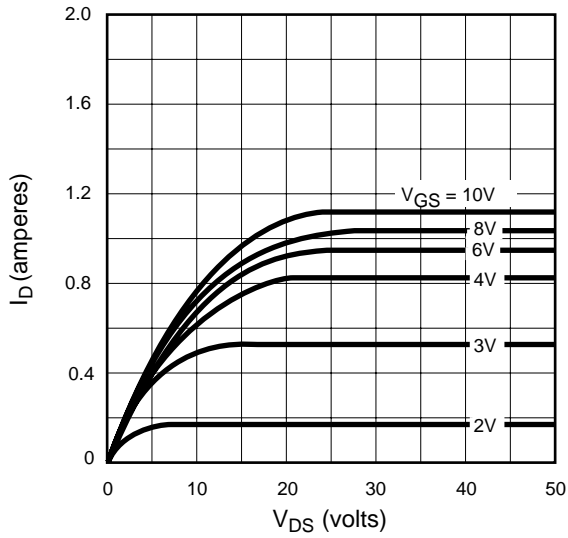
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

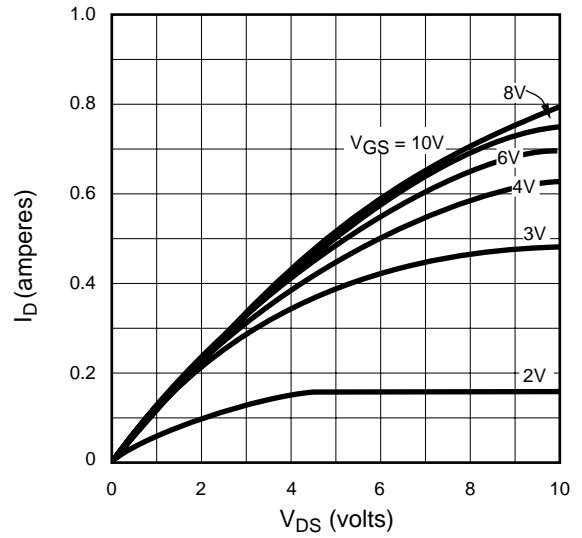


Typical Performance Curves

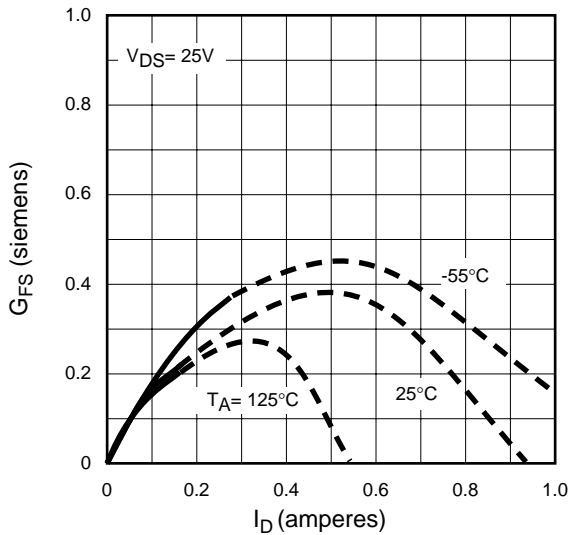
Output Characteristics



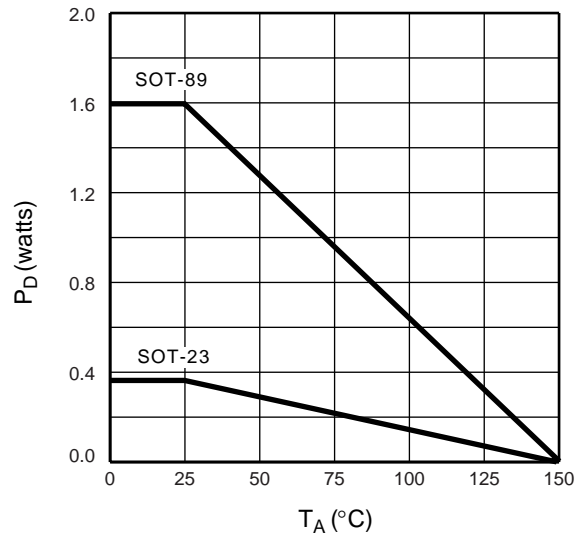
Saturation Characteristics



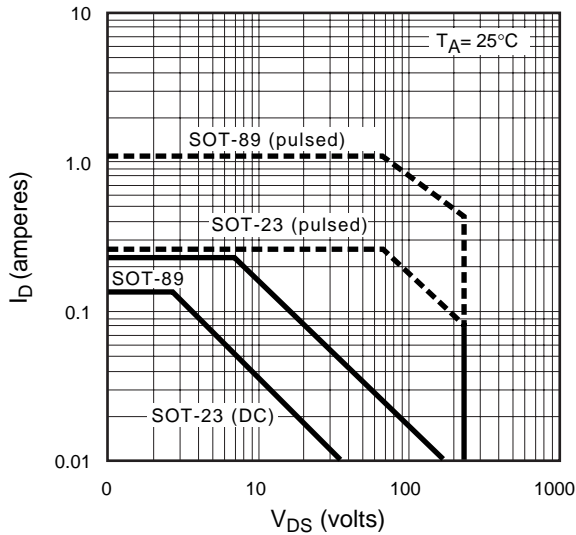
Transconductance vs. Drain Current



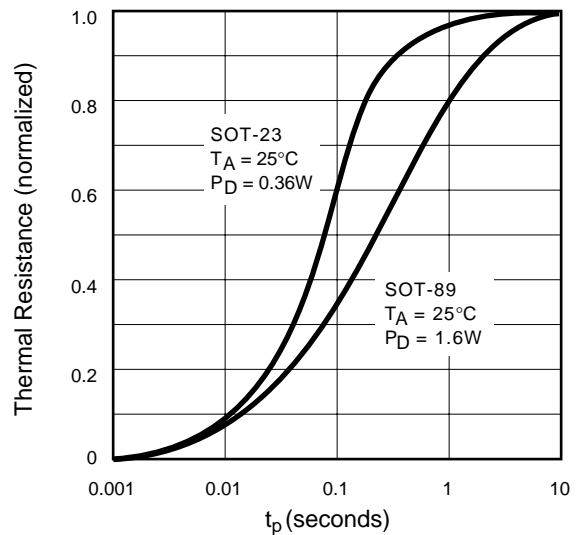
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

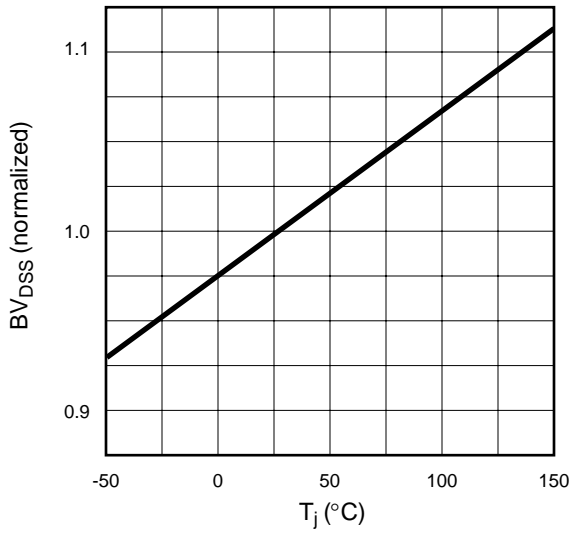


Thermal Response Characteristics

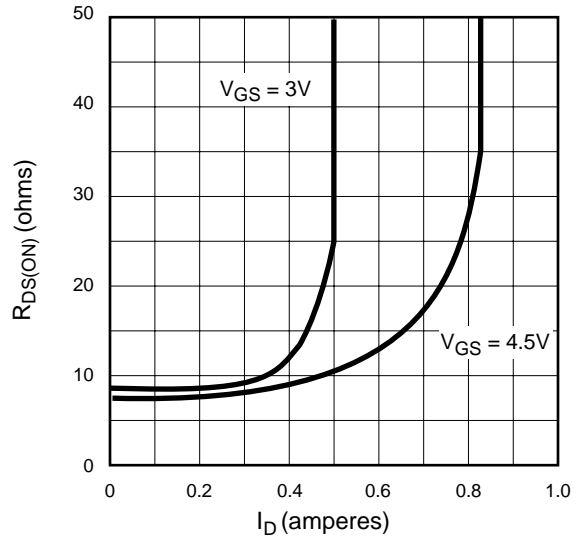


Typical Performance Curves

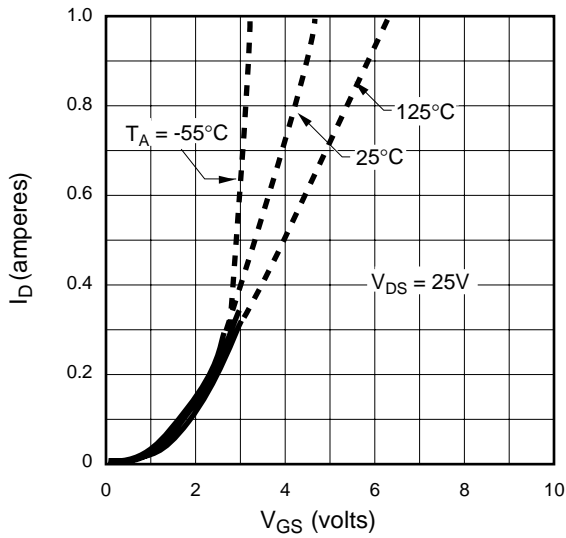
BV_{DSS} Variation with Temperature



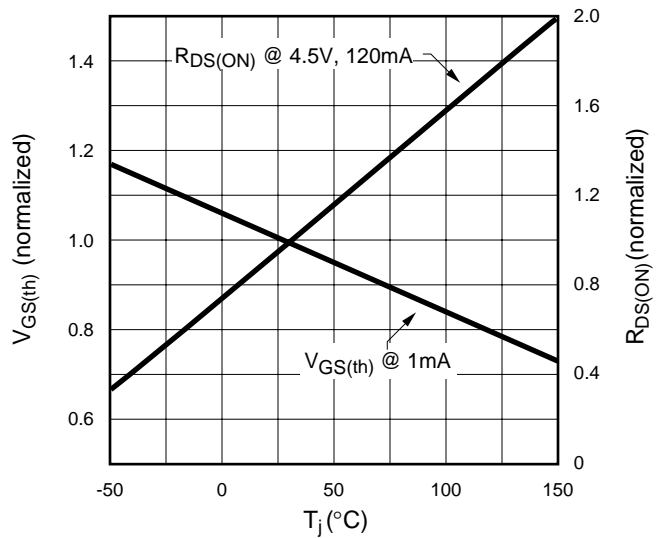
On-Resistance vs. Drain Current



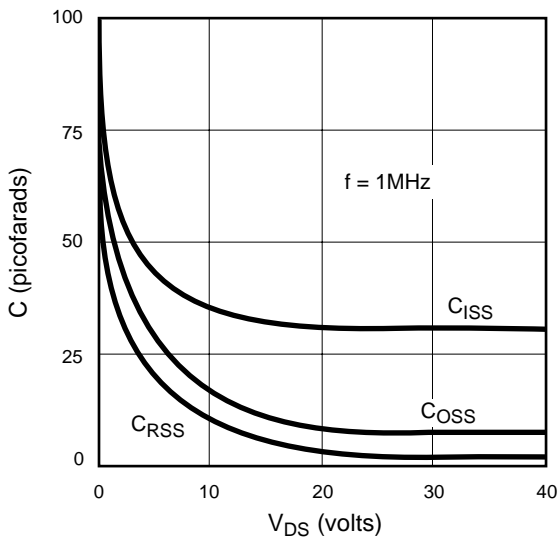
Transfer Characteristics



V_{TH} and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

