



**N-Channel Enhancement-Mode  
Vertical DMOS FETs**

**Ordering Information**

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package
				TO-243AA*
350V	10Ω	2.0V	1.0A	TN2535N8

\* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

**Features**

- Low threshold
- High input impedance
- Low input capacitance — 125pF max.
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

**Applications**

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

**Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

Product marking for TO-243AA

**TN5S\***

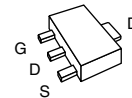
Where \* = 2-week alpha date code

**Low Threshold DMOS Technology**

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Package Option**



**TO-243AA  
(SOT-89)**

Note: See Package Outline section for dimensions.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-243AA	283mA	1.6A	1.6W <sup>†</sup>	15	78 <sup>†</sup>	283mA	1.6A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

<sup>†</sup> Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

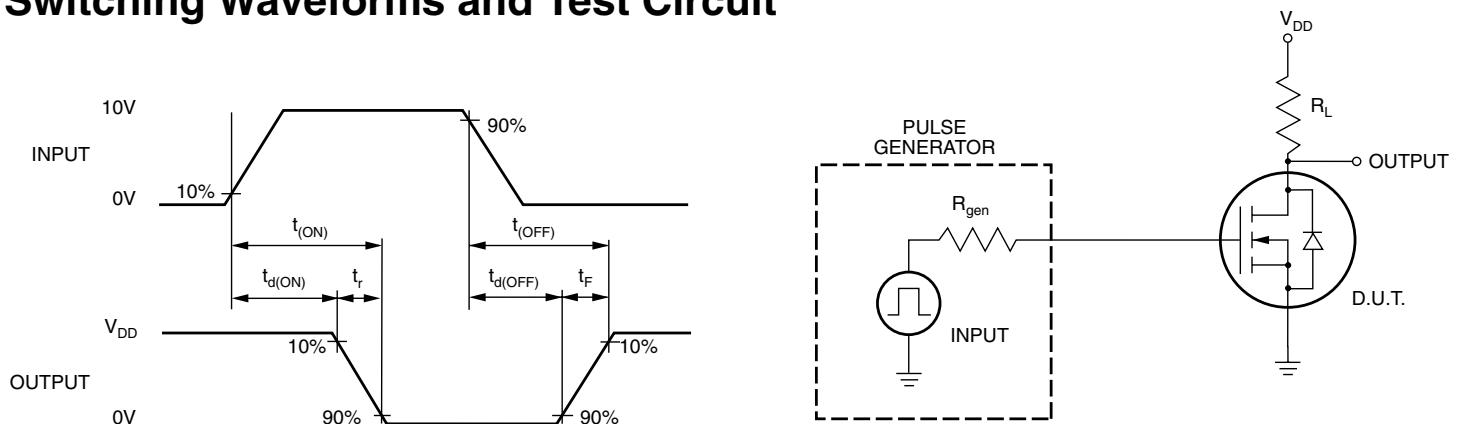
## Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$		350			V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	1.0		2.0	V	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			1.0	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
$I_{D(ON)}$	ON-State Drain Current	0.5			A	$V_{GS} = 4.5V, V_{DS} = 25V$
		1.0				$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			15	$\Omega$	$V_{GS} = 3.0V, I_D = 20\text{mA}$
				10		$V_{GS} = 4.5V, I_D = 100\text{mA}$
				10		$V_{GS} = 10V, I_D = 200\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 200\text{mA}$
$G_{FS}$	Forward Transconductance	125			m $\Omega$	$V_{DS} = 25V, I_D = 100\text{mA}$
$C_{ISS}$	Input Capacitance			125	pF	
$C_{OSS}$	Common Source Output Capacitance			70		
$C_{RSS}$	Reverse Transfer Capacitance			25		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	$V_{DD} = 25V,$ $I_D = 200\text{mA},$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
$t_f$	Fall Time			20		
$V_{SD}$	Diode Forward Voltage Drop			1.8	V	$V_{GS} = 0V, I_{SD} = 200\text{mA}$
$t_{rr}$	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = 200\text{mA}$

### Notes:

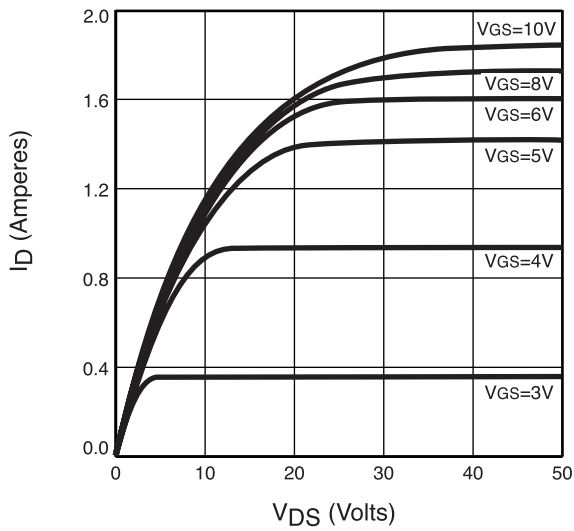
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

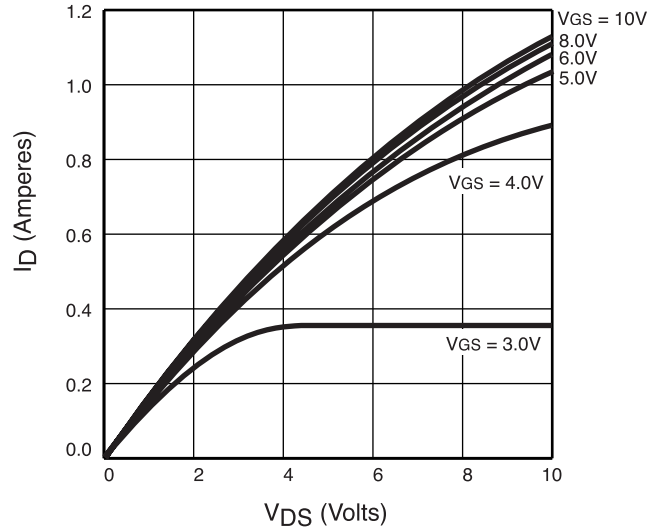


# Typical Performance Curves

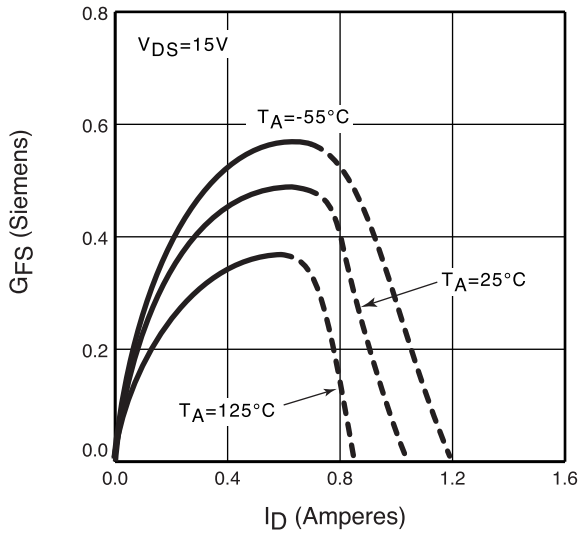
Output Characteristics



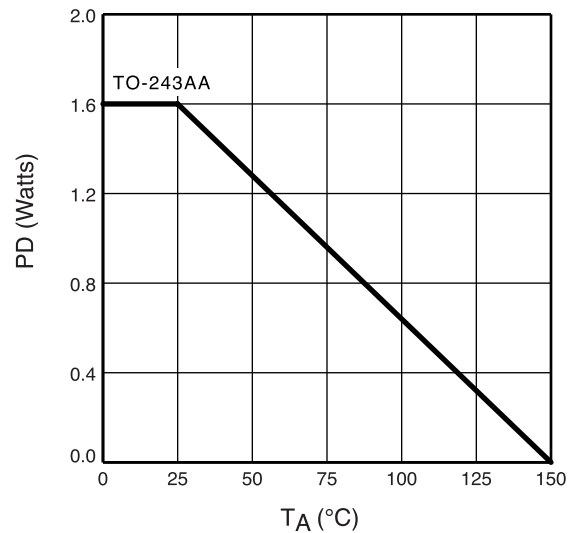
Saturation Characteristics



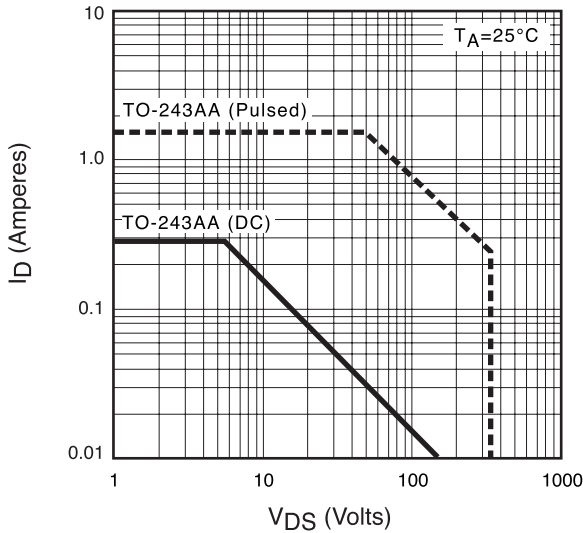
Transconductance vs. Drain Current



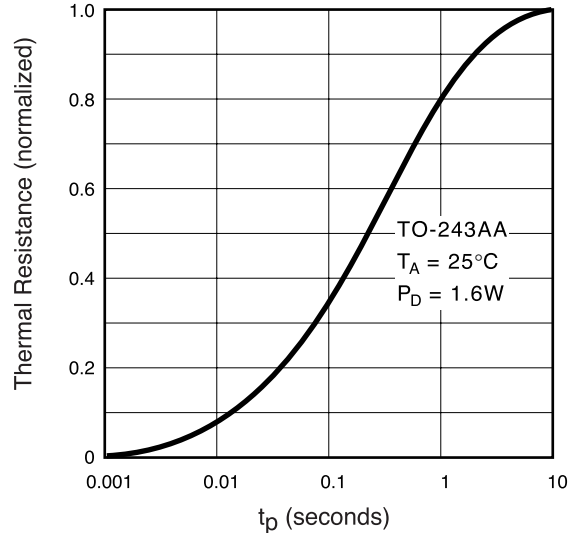
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



# Typical Performance Curves

