



## P-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package		
				SO-8	TO-92	Die†
-350V	15Ω	-2.0V	-0.7A	—	TP2635N3	—
-400V	15Ω	-2.0V	-0.7A	TP2640LG	TP2640N3	TP2640ND

†MIL visual screening available.

### Features

- Low threshold — -2.0V max.
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

### Low Threshold DMOS Technology

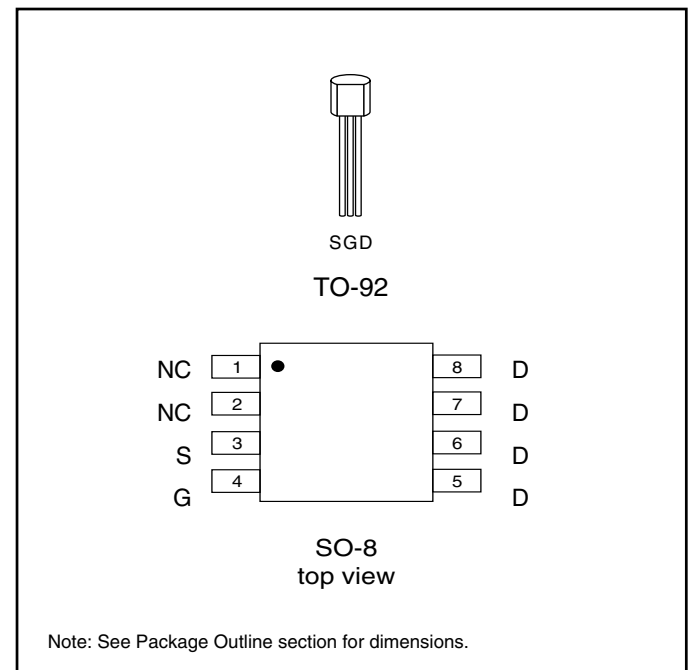
These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

### Package Options



### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

11/12/01

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
SO-8	-210mA	-1.25A	1.3W <sup>†</sup>	24	96 <sup>†</sup>	-210mA	-1.25A
TO-92	-180mA	-0.8A	1.0W	125	170	-180mA	-0.8A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

<sup>†</sup> Mounted on FR4 board, 25mm x 25mm x 1.57mm.

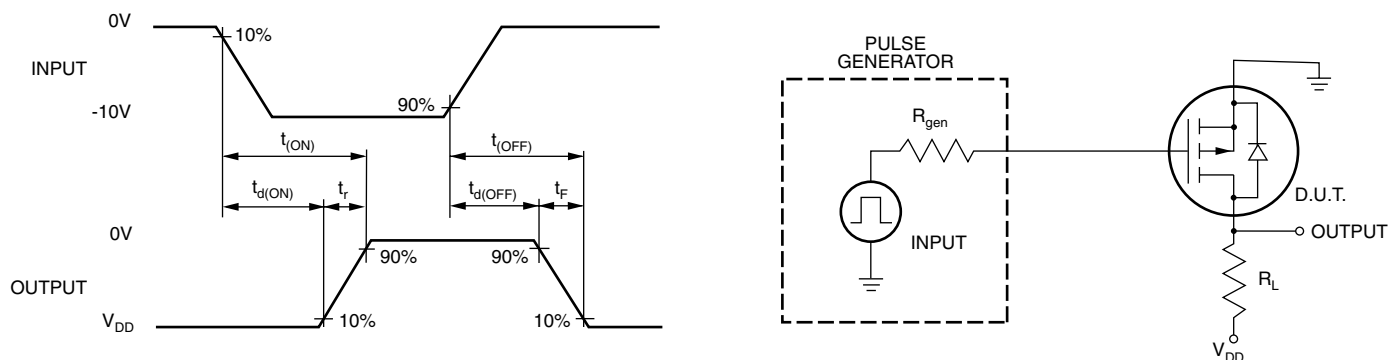
## Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	TP2640	-400			$V_{GS} = 0V, I_D = -2.0mA$
		TP2635	-350			
$V_{GS(th)}$	Gate Threshold Voltage	-0.8		-2.0	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
$I_{GSS}$	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			-1	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = -100V$
				-10	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				-1	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	0.7			A	$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		12	15		$V_{GS} = -2.5V, I_D = -20mA$
			11	15	$\Omega$	$V_{GS} = -4.5V, I_D = -150mA$
			11	15		$V_{GS} = -10V, I_D = -300mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -300mA$
$G_{FS}$	Forward Transconductance	200			m $\bar{S}$	$V_{DS} = -25V, I_D = -300mA$
$C_{ISS}$	Input Capacitance			300	pF	$V_{GS} = 0V, V_{DS} = -25V$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance			50		
$C_{RSS}$	Reverse Transfer Capacitance			12		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = -25V,$ $I_D = -300mA,$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			60		
$t_f$	Fall Time			40		
$V_{SD}$	Diode Forward Voltage Drop			-1.8	V	$V_{GS} = 0V, I_{SD} = -200mA$
$t_{rr}$	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = -200mA$

### Notes:

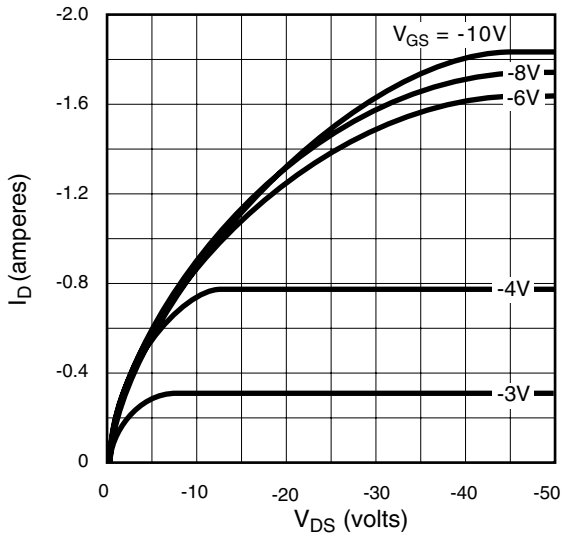
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

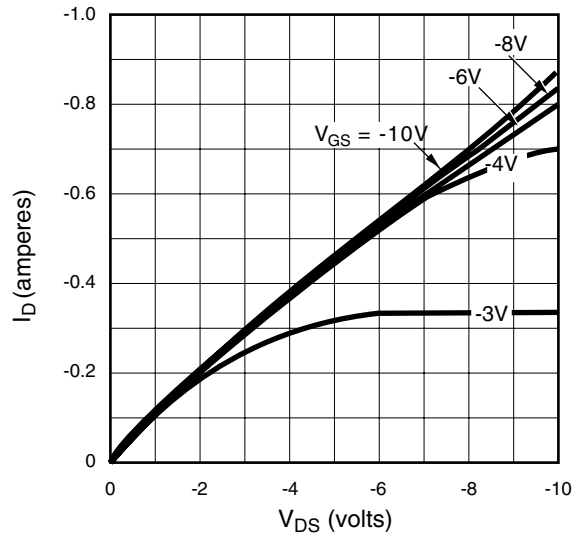


# Typical Performance Curves

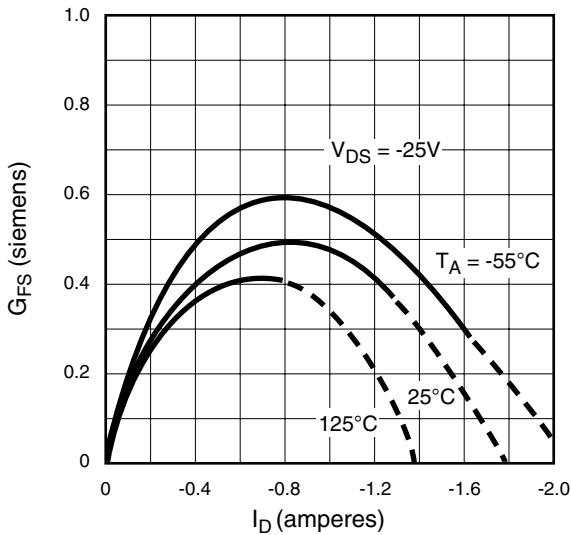
Output Characteristics



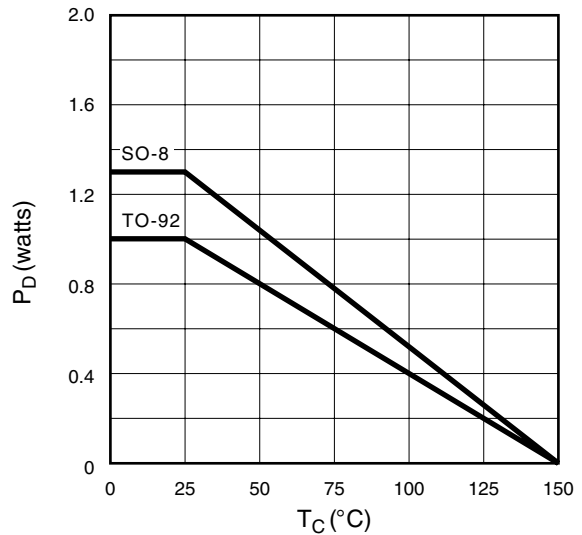
Saturation Characteristics



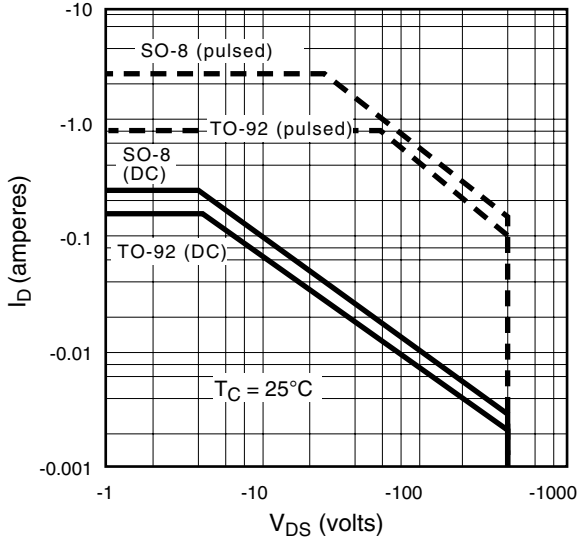
Transconductance vs. Drain Current



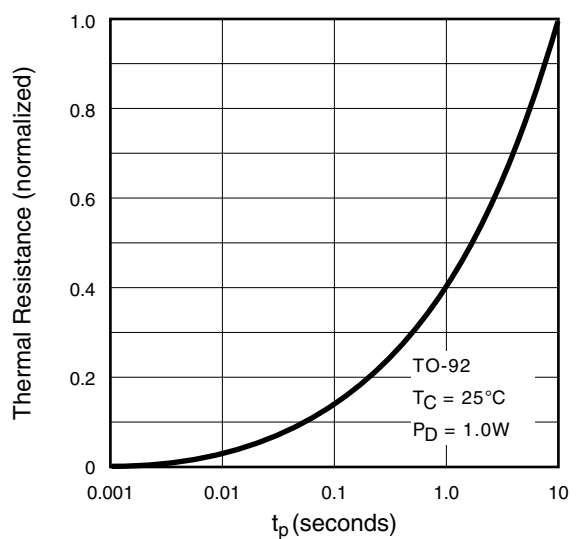
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

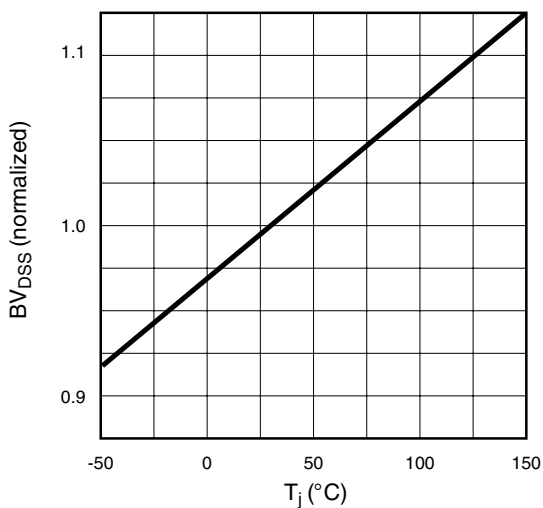


Thermal Response Characteristics

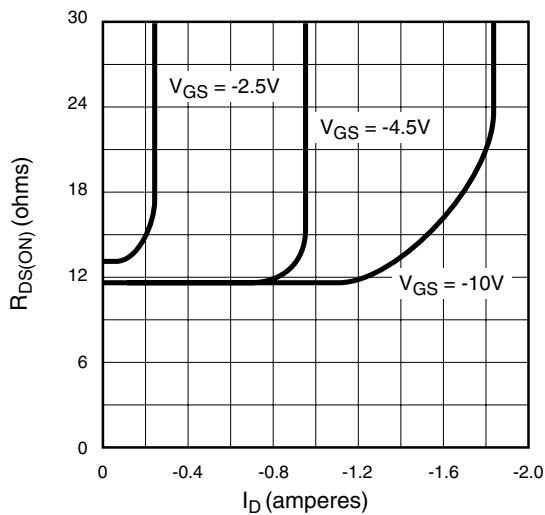


# Typical Curves

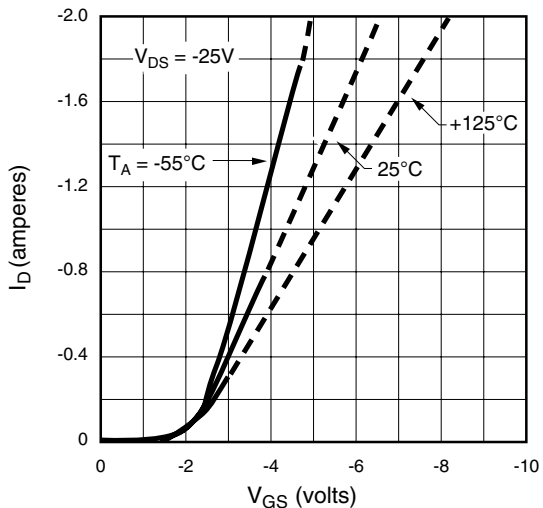
BV<sub>DSS</sub> Variation with Temperature



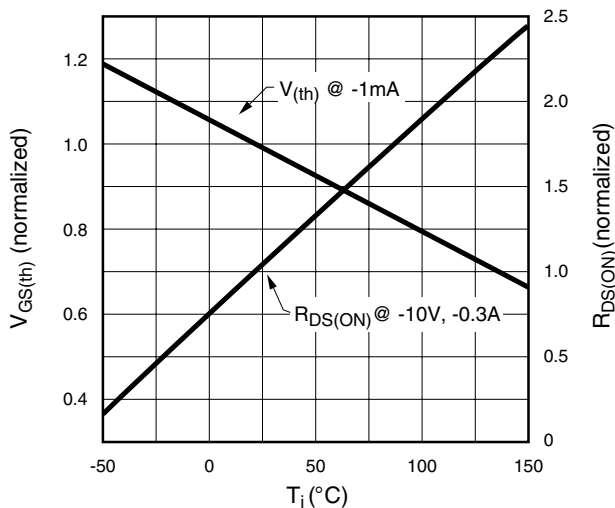
On-Resistance vs. Drain Current



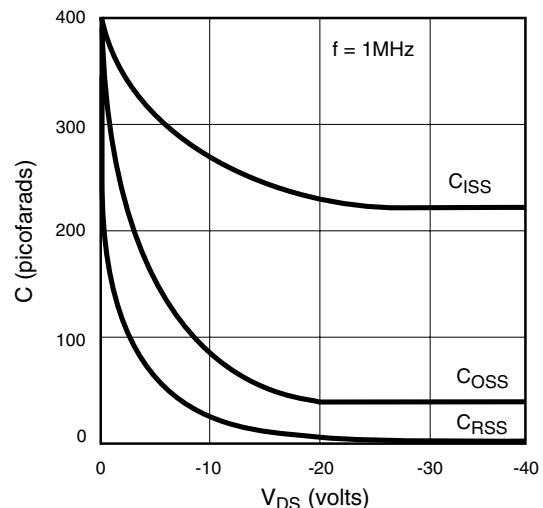
Transfer Characteristics



V<sub>TH</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

