V.22bis Single Chip Modem

Features

- **True one chip solution for embedded systems**
- **Low operating power**
  ~250mW @ 5V with standby and power down mode available
- **Designed for +5 volts (+/-10%)**
- **Data speed:**
  V.22bis – 2400bps
  V.22/Bell212 – 1200bps
  V.21/Bell103 – 300bps
  V.23 – 1200/75bps (with PAVI turnaround)
  Bell202 – 1200bps
  Bell202/V23 4-wire operations
- **International Call Progress support**
  FCC68, CTR21, JATE, etc.
- **Worldwide Caller ID capability**
- **DTMF generation and detection**
- **On chip hybrid driver**
- **Blacklisting capability**
- **Line-In-Use and Parallel Pick-Up (911) detection capability**
- **Manufacturing Self Test capability**
- **Packaging:**
  32 pin PLCC / 44 pin TQFP

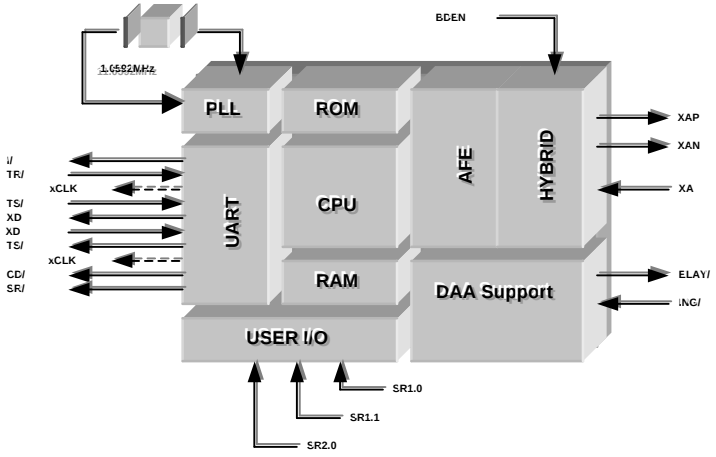
Applications

Set Top Box
Point of Sale Terminal
Automatic Teller Machine
Hand Held communication Device
Metering Device
Vending Machine
Credit Card Reader

Description

The 73M2901C/5V is a single-chip modem that combines all the controller (DTE) and data pump functions necessary to implement an intelligent V.22bis data modem. This device is based on TDK Semiconductor's implementation of the industry standard 8032 microcontroller core with a proprietary multiply and accumulate (MAC) coprocessor; Sigma-Delta A/D and D/A converters; and an analog front end. The ROM and RAM necessary to operate the modem are contained in the device. Additionally, the 73M2901C/5V provides an on-chip oscillator and Hybrid driver.

Block Diagram



Hardware Description

The 73M2901C/5V is designed for a single +5 volt supply with low power consumption (~250mW @ 5 volts). The modem supports automatic standby idle mode. The modem will also accept a request to power down from the DTE via hardware control. No additional major components are required to complete the modem core logic. The modem provides direct firmware LED support via port pins.

HARDWARE FEATURES

- Fully self-contained "AT" Command interpreter and data pump
- User pins available
- Synchronous serial data I/O available
- Asynchronous serial port
- On-chip hybrid driver.
- Autobaud capability from 300bps to 9600bps

POWER SUPPLY

Power is supplied to the 73M2901C/5V via the VPD and VPA pins. The 73M2901C/5V is designed for a single 5 volt (+/-10%) supply and for low power consumption (~250mW @ 5 volts). Ground Reference is provided at the VND and VNA pins.

LOW POWER MODE

The TDK 73M2901C/5V supports a low power standby mode. If the low power standby option is enabled the 73M2901C/5V will go into a power saving mode when idle. The oscillator will be running, clocks will be supplied to the UART, timers and interrupt blocks; but no clocks will be supplied to the CPU. Instruction processing and activity on the internal busses is halted. Normal operation is resumed when an interruption such as assertion of $\overline{DTR}$ or $\overline{RING}$, any character is sent to the 73M2901C/5V, or when a reset occurs.

ANALOG LINE / HYBRID INTERFACE

The 73M2901C/5V provides a differential analog output (TXAP and TXAN) and a single-ended analog input (RXA) with internal A/D and D/A converters. A driver is provided for an internal hybrid function.
The internal hybrid driver is capable of driving an external load matching impedance and a line-coupling transformer. If an external hybrid is to be used, the on-chip hybrid drivers can be reconfigured to drive a minimum load of 50kΩ and thus reduce the driver's power consumption.
The hybrid configuration is controlled by the state of the HBDEN pin. For driving a line-coupling transformer, HBDEN should be pulled high. For driving an external hybrid (load on TXAP and TXAN is 50kΩ or larger), HBDEN should be pulled low.
The 73M2901C/5V provides firmware control for a hook relay driver ($\overline{RELAY}$) as well as interrupt support for a ring detect opto-coupler ($\overline{RING}$).

INTERRUPT PINS

The external interrupt sources, $\overline{DTR}$ and $\overline{RING}$, come from dedicated input pins of the same name.
$\overline{DTR}$ informs the 73M2901C/5V that the host has requested the 73M2901C/5V perform a specific function. The actual particulars of that function can be changed by "AT" commands (described in full in the TDK 73M2901C User's Guide).
$\overline{RING}$ is used to inform the 73M2901C/5V that the external DAA circuitry has detected a ring signal.
In addition, sending any character on the TXD line also generates an internal interrupt.

CRYSTAL OSCILLATOR

The TDK 73M2901C/5V single chip modem can use an external 11.0592 MHz reference clock or can generate such a clock using only a crystal and two capacitors. If an external clock is used, it should be applied to OSCIN.

SPECIFYING A CRYSTAL

The manufacturer of a crystal resonator verifies its frequency of oscillation in a test set-up, but to ensure that the same frequency is obtained in the application, the circuit conditions must be the same. The TDK 73M2901C/5V modem requires a parallel mode (anti-resonant) crystal, the important specifications of which are as follows:

Mode: Parallel (anti-resonant)
Frequency: 11.0592 MHz
Frequency tolerance:
±50 ppm at initial temperature.
Temperature drift:
±50 ppm additional over full Range.
Load capacitance: 18pF or 20pF
ESR: 75Ω max.
Drive level: Less than 1mW.

RESET

A reset is accomplished by holding the RESET pin high. To ensure a proper power-on reset, the reset pin must be held high for a minimum of 3µs. At power on, the voltage at VPD, VPA, and RESET must come up at the same time for a proper reset. The signals $\overline{DCD}$, $\overline{CTS}$ and $\overline{DSR}$ will be held inactive for 25ms, acknowledging the reset operation, within a 250ms time window after the reset triggering event. The 73M2901C/5V is ready for operation after that 250ms windows and/or after the signals $\overline{DCD}$, $\overline{CTS}$ and $\overline{DSR}$ become active.

ASYNCHRONOUS AND SYNCHRONOUS SERIAL DATA INTERFACE

The serial data interface consists of the TXD and RXD data paths (LSB shifted in and out first, respectively); and the TXCLK and RXCLK serial clock outputs associated with the data pins; $\overline{CTS}$/$\overline{RTS}$ flow control; $\overline{DCR}$, $\overline{DSR}$ and $\overline{DTR}$. In synchronous mode, the data is passed at the bit rate (tolerance is +1%, -2.5%)

Pin Descriptions

POWER PIN DESCRIPTION

PIN NAME	32 pin PLCC	44 pin TQFP	TYPE	DESCRIPTION
VPA	15	16	I	Positive analog voltage (Analog supply)
VNA	21	22	I	Negative analog voltage (Analog ground)
VPD	6, 25, 29	2, 12, 27, 33	I	Positive digital voltage (Digital supply)
VND	5, 22, 26	11, 24, 44, 28	I	Negative digital voltage (Digital ground)

ANALOG INTERFACE PIN DESCRIPTION

PIN NAME	32 pin PLCC	44 pin TQFP	TYPE	DESCRIPTION
RXA	20	21	I	Receive analog data
TXAN	16	17	O	Transmit Analog-
TXAP	17	18	O	Transmit Analog+
HBDEN	14	15	I	2w/4w hybrid driver enable pin 0=Driver configure for 50kΩ or greater load (tie to VND) 1=Driver configured for driving line-coupling transformer (tie to VPD)
VBG	19	20	O	Analog Band Gap voltage reference (0.1µF to VNA). This pin must not be connected to another external circuitry other than the decoupling capacitor.
VREF	18	19	O	Analog reference voltage (0.1µF to VNA)

DIGITAL INTERFACE PIN DESCRIPTION

PIN NAME	32 pin PLCC	44 pin TQFP	TYPE	DESCRIPTION
RESET	13	9	I	Reset
RXCLK	31	36	O	Receive data synchronous clock
RXD	30	35	O	Serial output to DTE
TXCLK	28	31	O	Transmit data synchronous clock
TXD	27	30	I	Serial data input from DTE
USR10	12	8	I/O	Programmable I/O port. This pin can optionally be used to control an external switch for caller ID operations or external Line In Use or Parallel Pick Up circuitry.
USR11	11	7	I/O	Programmable I/O port. This pin can optionally be used to control an external switch for caller ID operations or external Line In Use or Parallel Pick Up circuitry.
$\overline{\text{RTS}}$	10	6	I	Request to send
$\overline{\text{CTS}}$	9	5	O	Clear to send
$\overline{\text{DSR}}$	8	4	O	Data set ready
$\overline{\text{DCD}}$	7	3	O	Data carrier detect
$\overline{\text{RI}}$	4	43	O	Ring indicator
$\overline{\text{RELAY}}$	3	40	O	Relay driver output
USR20	1	38	I/O	Programmable I/O port

EXTERNAL INTERRUPTS PIN DESCRIPTIONS

PIN NAME	32 pin PLCC	44 pin TQFP	TYPE	DESCRIPTION
$\overline{\text{RING}}$	2	39	I	External interrupt – Line interface ring detection circuitry input
$\overline{\text{DTR}}$	32	37	I	External interrupt – DTE DTR signal input

OSCILLATOR PIN DESCRIPTION

PIN NAME	32 pin PLCC	44 pin TQFP	TYPE	DESCRIPTION
OSCIN	24	26	I	Crystal input for internal oscillator, also input for external source
OSCOUT	23	25	O	Crystal oscillator output

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

Operations above maximum rating may permanently damage the device.

PARAMETER	RATING
Supply Voltage	-0.5V to +7.0V
Pin Input Voltage	-0.5V to VPD + 0.5V
Storage Temperature	-55ºC to 150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage	+5V (+/-10%)
Oscillator Frequency	11.0592MHz +/- 50ppm
Storage Temperature	-40ºC to 85ºC

RECEIVER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Carrier detect On	Tip and Ring			-43	dBm0[1]
Carrier detect Off	Tip and Ring	-48			dBm0[1]
Carrier Detect Hysteresis	Tip and Ring		2		dB
Receive Level	Tip and Ring	-43		-9	dBm0[1]
Idle channel noise	0.2KHz – 4.0KHz		-70	-65	dB
Input impedance	RXA	150			kΩ
Receive Gain Boost	SFR 96h bit 2(Rxgain)=1	17.75		20.75	dB
Maximum Input Level at RxA	Vref=1.25V			0.587	Vpk
	Vref=2.25V			1.069	Vpk
Total Harmonic Distortion (THD)	1KHz 450mVpk on RXA THD=2nd and 3rd harmonic		-70	-50	dB

TRANSMITTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ITU Guard tone power	550Hz (relative to carrier)	-5	-3.5	-2	dB
	1800Hz (relative to carrier)	-8	-6.5	-5	dB
Calling Tone transmit power	1300Hz		-11.5		dBm0[1]
Answer Tone transmit power	2225Hz/2100Hz		-11		dBm0[1]
Transmit tolerance, all tones and carriers		-1.2		1.2	dB
TX boost, carrier or DTMF	ATS73+128 or ATS92+2	4.7	5	5.3	dB
Gain adjust tolerance	By step (ATS13)	-0.3	0	0.3	dBm0[1]
Total Harmonic Distortion (THD)	1KHz sine wave at output (TXAP-TXAN) 1.5Vpk(2.7dBm) for Vref=1.25V 2.4Vpk(6.8dBm) for Vref=2.25V THD=2nd and 3rd harmonic			-50	dB
Intermod Distortion	At output (TXAP-TXAN) 1KHz, 1.2KHz sine waves summed 2Vpk for Vref=1.25V 2.4Vpk for Vref=2.25V	Each unwanted frequency component		-33	dBm
		Sum of unwanted frequency components in pass band		-20	dB below low tone
Power supply rejection ratio	-30dBm signal at VPA 300Hz-30KHz. Measured TXAP to TXAN			30	dB

DATA SHEET

[1] dBm0 refers to the TDK recommended line interface (8dB loss from transmit pins to the line and 5dB loss from the line to the receiver pin). Results may vary depending on selected DAA. 0dBm=0.775mV$_{rms}$; dBm=10log(V$_{rms}^2$/(1mW)(600Ω))

NOMINAL TRANSMIT LEVELS	CONDITIONS	MAX	UNIT
QAM	Vref=1.25V S73=48	-13.3	dBm0[1]
	Vref=2.25V S73+128	-8.3	dBm0[1]
DPSK	Vref=1.25V S73=48	-13.3	dBm0[1]
	Vref=2.25V S73+128	-8.3	dBm0[1]
FSK	Vref=1.25V S73=48	-11	dBm0[1]
	Vref=2.25V S73+128	-6	dBm0[1]
DTMF (HIGH TONE)	Vref=1.25V S92=4	-11.5	dBm0[1]
	Vref=2.25V S92+2	-6.5	dBm0[1]
DTMF (LOW TONE)	Vref=1.25V S92=4	-13	dBm0[1]
	Vref=2.25V S92+2	-8	dBm0[1]
DTMF (TOTAL)	Vref=1.25V S92=4	-6.7	dBm0[1]
	Vref=2.25V S92+2	-1.7	dBm0[1]

DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input low voltage (except OSCIN, RESET)	VIL		-0.5		0.2Vcc	V
Input low voltage OSCIN, RESET	VIL		-0.5		0.2Vcc	V
Input high voltage (except OSCIN, RESET)	VIH		0.5Vcc		Vcc+0.5	V
Input high voltage OSCIN, RESET	VIH		0.7Vcc		Vcc+0.5	V
Output low voltage (except OSCOUT)	VOL	IOL=4mA			0.45	V
Output low voltage OSCOUT	VOLOSC	IOL=3mA			0.7	V
Output high voltage (except OSCOUT)	VOH	IOH=-4mA	Vcc-0.45			V
Output high voltage OSCOUT	VOHOSC	IOH=-3mA	Vcc-0.9			V
Input leakage current (except OSCIN)	IIH	Vss<Vin<Vcc			1	µA

Input leakage current OSCIN	IIH	Vss<Vin<Vcc	1		30	µA
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**NOM**	**MAX**	**UNIT**
Maximum Power supply, normal operation, HBDEN pulled high	IDD1	30pF/pin		51	62	mA
Maximum Power supply, normal operation, HBDEN pulled low	IDD1	30pF/pin		35	43	mA
Maximum digital power	IDDd	30pF/pin		31	37	mA
Maximum analog power, HBDEN pulled high	IDDah1	30pF/pin		20	25	mA
Maximum analog power, HBDEN pulled low	IDDah0	30pF/pin		4	6	mA
Maximum power supply Idle mode	IDD2	30pF/pin		11	15	mA
Maximum power supply Power down mode	IDD3	30pF/pin		4	10	µA

PARAMETER	**CONDITIONS**	**MIN**	**NOM**	**MAX**	**UNIT**
Vbg	Vcc=5V	1.19	1.25	1.31	V
Vref	Vcc=5V	1.19	1.25	1.31	V
	Vcc=5V + internal boost	2.14	2.25	2.36	V

Firmware Description[2]

An "AT" command interpreter provides command and configuration of the 73M2901C/5V. This provides the user a uniform interface to control the modem in embedded applications.

The signal processing is performed by obtaining data from and providing data to the integrated A/D converter. A MAC hardware processor is provided for computation.

To provide maximum flexibility, the system host processor can access the internal RAM and Control Register space in the modem. This will allow the OEM user to modify parameters such as filter response, transmit levels through the AT command set using proprietary commands. The host processor can also access the modem I/O port pins, providing extended I/O capability.

FIRMWARE REQUIREMENTS

The modem always powers up in the idle (on hook) mode. "AT" commands are issued via the serial interface from the host. All modem configuration commands are received in this manner. The data modem firmware is contained in an internal ROM. The firmware will automatically enter a power saving idle mode if the modem is on hook and there are no incoming host commands. The modem automatically powers up upon receiving the next command. This power up sequence occurs without delay to the host. This function, while saving power, is transparent to the host processor and can be disabled by the host via an "AT" command. The host can also program the modem to power down via external pin ($\overline{DTR}$) or via a firmware command.

FIRMWARE FEATURES

- "AT" command set
- Supports data standards through V.22bis
- Provides DAA control firmware (e.g. ring detect, hook control)
- Multinational Call progress support (FCC68, CTR21, JATE…)
- Caller ID capability
  - *FSK demodulation (V23 or Bell202)*
  - *DTMF demodulation*
  - *Intra 1st/2nd ring CID data operations*
  - *Post Line reversal CID data operations*
- On hook Line-In-Use detection support (No line seizure will occur when a Line-In-Use condition is detected)
  - *Tip/Ring voltage sensing*
  - *Quiescent line validation*
- Off hook Parallel Pick-Up detection support (Line seizure will be aborted as soon as a Parallel Pick-Up condition is detected)
  - Loop current variation sensing
- Interfaces with standard V.24/EIA-232 (5V inverted level) serial interface using the built in serial port and firmware control of port pins
- Provides tone generation and detection, four imprecise and four precise call progress detect filters
- Blacklisting capability
- Host access to program RAM provided
- User access to modem function
- Bell 212A fast connect

[2] Refer to the TDK 73M2901C User Guide for a complete description of the software.

Design Considerations

TDK Semiconductor's single chip modem solutions include all the basic modem functions. This makes these devices adaptable to a variety of applications.
Unlike digital logic circuitry, modem designs must contend with precise frequency tolerances and verify low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. The crystal oscillator should be held to a 50ppm tolerance. Following are additional recommendations that should be taken into consideration when starting new designs.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain high performance in modem designs. The more digital circuitry present in the application, the more attention to noise control is needed.
High speed, digital devices should be locally bypassed, and the telephone line interface and the modem should be located next to each other near where the telephone line connection is accessed. It is recommended that power supplies and ground traces should be routed separately to the analog and digital portions on the board. Digital signals should not be routed near low level analog or high impedance analog traces.
The 73M2901C/5V should be considered a high performance analog device. A 10µF electrolytic capacitor in parallel with a 0.1µF Ceramic capacitor should be placed between VPD and VND as well as between VPA and VNA. A 0.1µF ceramic capacitor should be placed between VREF and VNA as well as VBG and VNA. Use of ground planes and large traces on power is recommended.

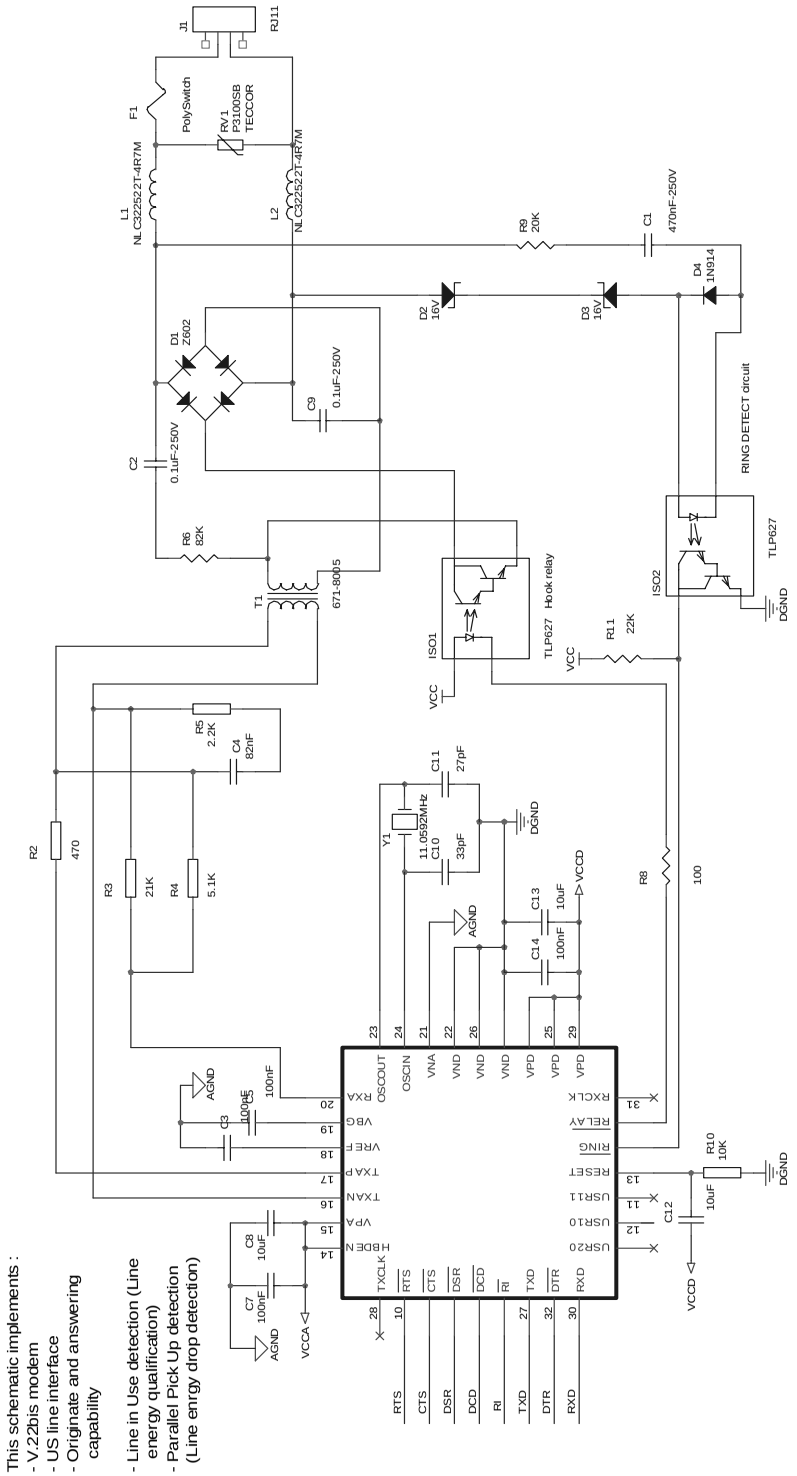
73M2901 DESIGN COMPATIBILITY

The TDK 73M2901C is an enhanced version of the TDK 73M2901 and has a number of new features. Although the two parts are highly compatible, special attention should be paid when changing an existing 73M2901 design to use the 73M2901C. From a hardware standpoint, the key differences involve the User I/O pins USR10 and USR11, and the $\overline{\text{ASRCH}}$ pin which has been removed and replaced by USR20. In an existing 73M2901 design, pin USR20 of the TDK 73M2901C can safely remain connected to TXD as long as no modification on the user I/O is performed by the host software (S103, S104). The functions of USR10 and USR11 are related to Caller ID and Line In Use/Parallel Pickup support.
Software enhancements to the 73M2901C are typically achieved by the addition of new AT commands and so the device can be considered a superset of the 73M2901. However, the user should check all AT commands and register settings for compatibility with the intended application (refer to the TDK 73M2901C User Guide for complete details).

TELEPHONE LINE INTERFACE

Transmit levels at the line are dependent on the interface used between the pins and the line. Drivers are provided to drive the line coupling transformer directly without the need for external drivers or hybrid circuitry. TXAP and TXAN can be connected directly to the transformer through the required impedance matching series resistor.
The line interface circuit shown on the following page represents the basic components and values for interfacing the TDK 73M2901C/5V analog pins to the telephone line.

TYPICAL USA APPLICATION SCHEMATIC



Modem Performance Characteristics

The curves presented in this data sheet define modem IC performance under a variety of line conditions typical of those encountered over public service telephone lines.

BER vs. SNR

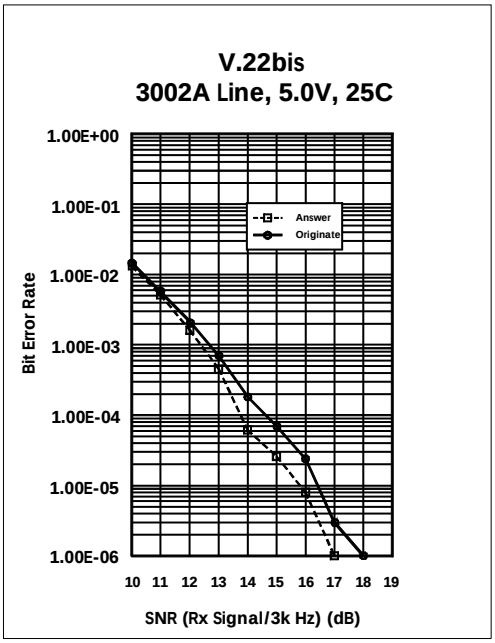
This test represents the ability of the modem to operate over noisy lines with a minimum amount of data transfer errors. Since some noise is generated in the best dial up lines, the modem must operate with the lowest signal to noise ratio (SNR) possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically a DPSK modem will exhibit better BER performance test curves receiving in the low band (answer mode) than in the high band (originate mode).

BER vs. RECEIVE LEVEL

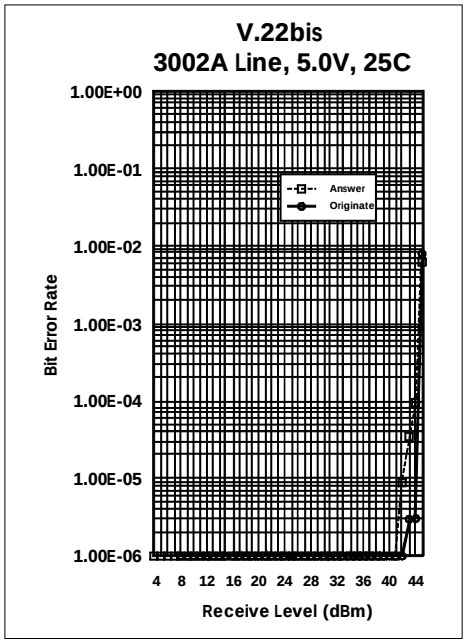
This test measures the dynamic range of the modem. Because signal levels vary widely over dial up lines, the widest possible dynamic range is desirable. The SNR is held constant at the indicated values as the Receive level is lowered from very a very high to a very low signal level. The width of the bowl of these curves, taken at the BER point is the measure of the dynamic range.

BER Curves

BER vs SNR



BER vs Receive Level



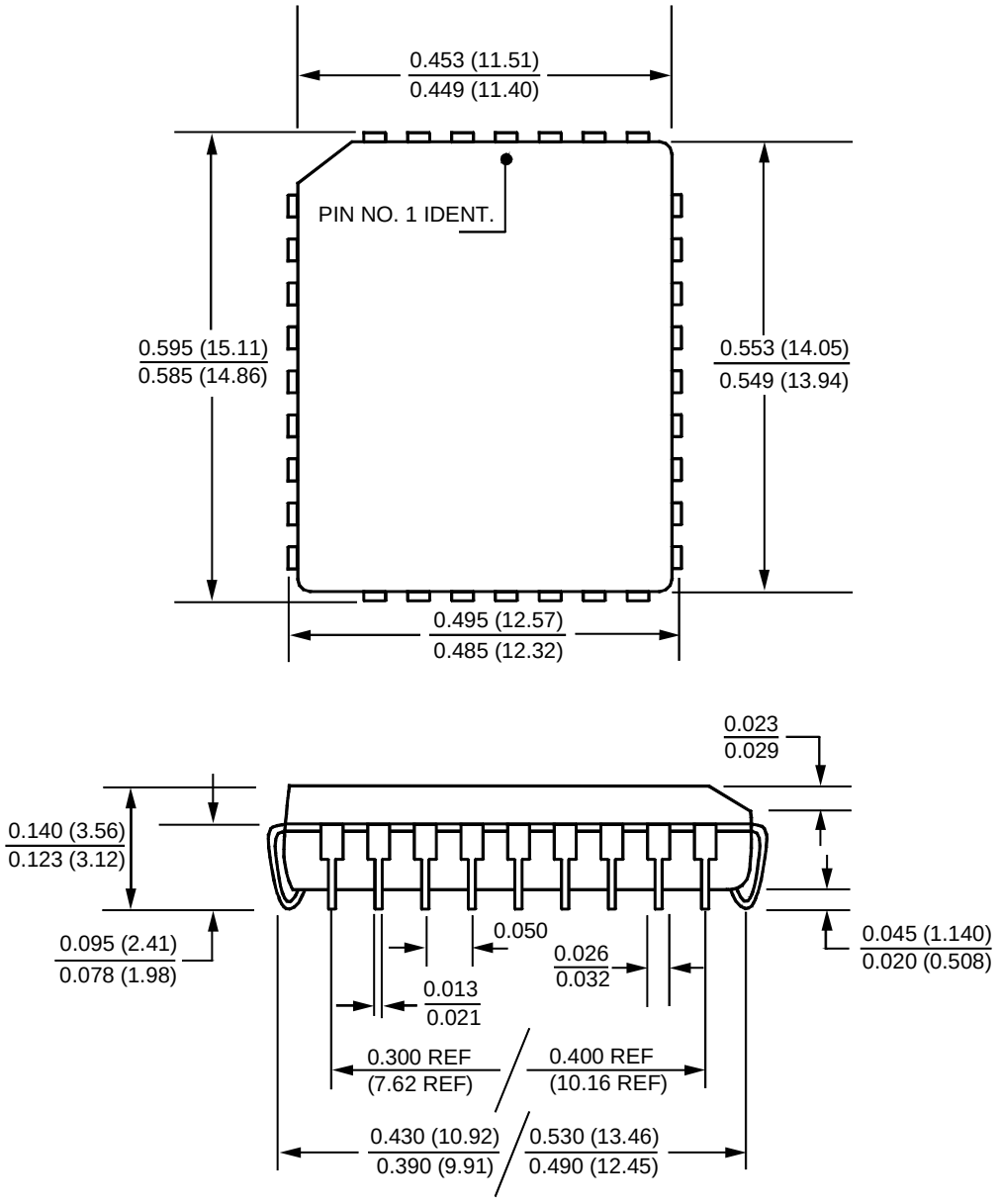
32 PIN PLCC PIN-OUT

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	USR20	9	CTS	17	TXAP	25	VPD
2	RING	10	RTS	18	VREF	26	VND
3	RELAY	11	USR11	19	VBG	27	TXD
4	RI	12	USR10	20	RXA	28	TXCLK
5	VND	13	RESET	21	VNA	29	VPD
6	VPD	14	HBDEN	22	VND	30	RXD
7	DCD	15	VPA	23	OSCOUT	31	RXCLK
8	DSR	16	TXAN	24	OSCIN	32	DTR

44 PIN TQFP PIN-OUT

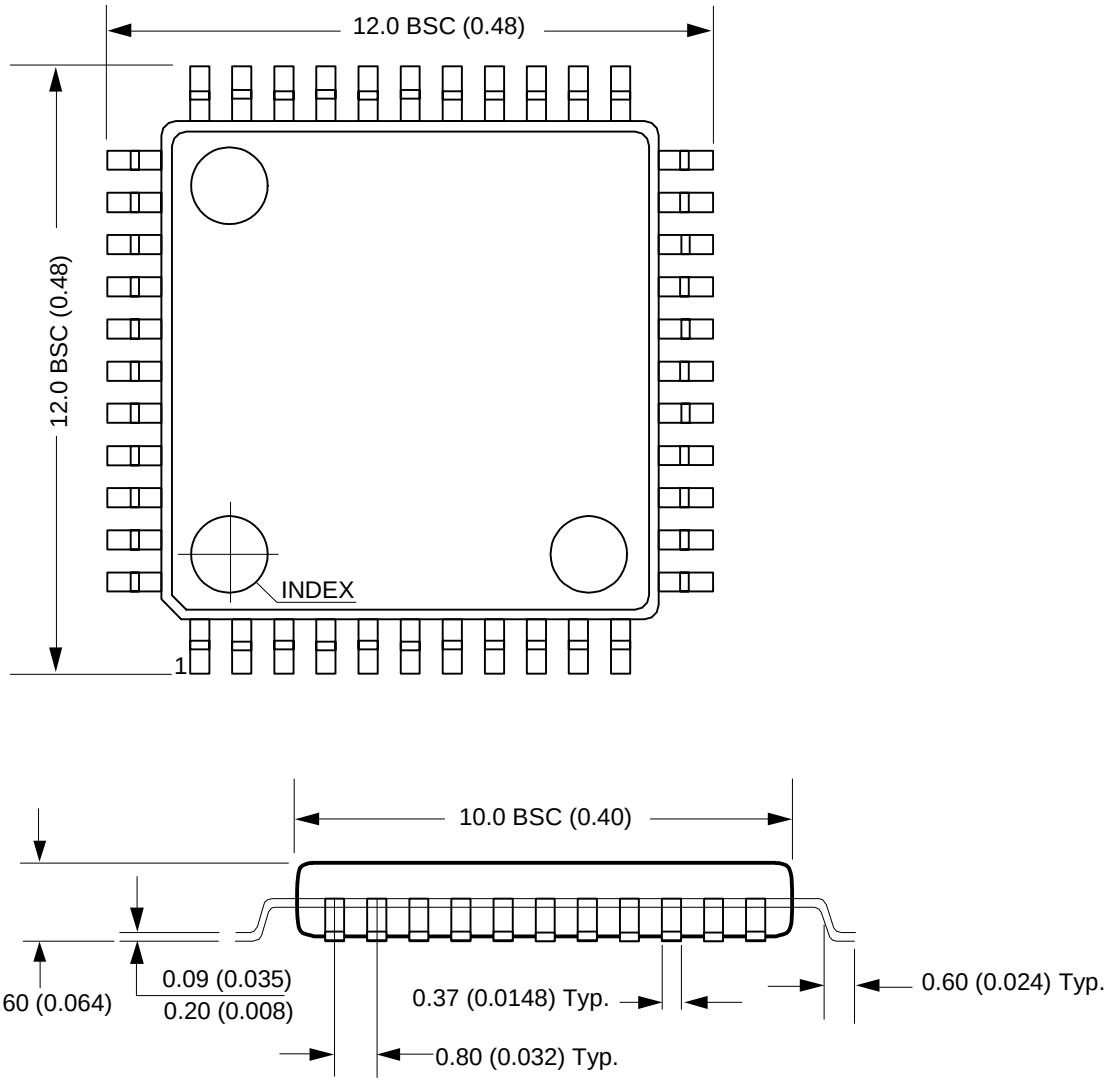
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	N/C	12	VPD	23	N/C	34	N/C
2	VPD	13	N/C	24	VND	35	RXD
3	DCD	14	N/C	25	OSCOUT	36	RXCLK
4	DSR	15	HBDEN	26	OSCIN	37	DTR
5	CTS	16	VPA	27	VPD	38	USR20
6	RTS	17	TXAN	28	VND	39	RING
7	USR11	18	TXAP	29	N/C	40	RELAY
8	USR10	19	VREF	30	TXD	41	N/C
9	RESET	20	VBG	31	TXCLK	42	N/C
10	N/C	21	RXA	32	N/C	43	RI
11	VND	22	VNA	33	VPD	44	VND

MECHANICAL DRAWINGS



32 pin PLCC

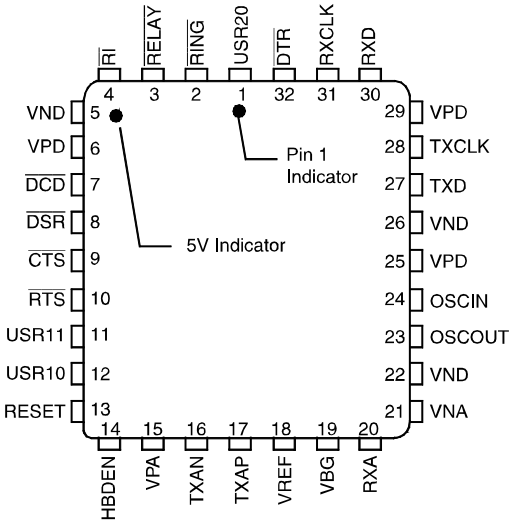
DATA SHEET



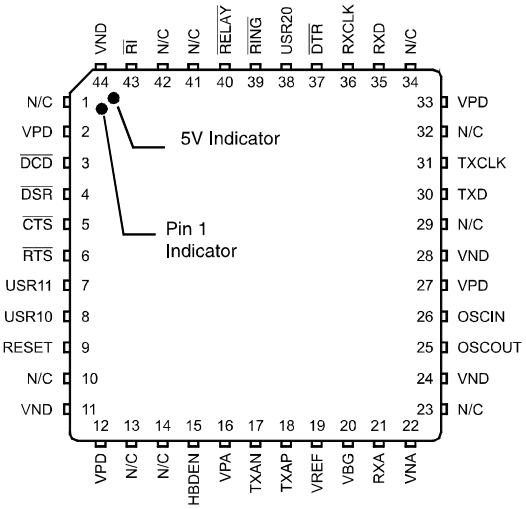
44 pin TQFP (JEDEC LQFP)

DATA SHEET

PACKAGE PIN DESIGNATIONS (TOP VIEW)



32-Lead PLCC
73M2901C-32IH



44-Pin TQFP
73M2901C-IGT

Ordering Information

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
73M2901C 32-Pin Plastic Leaded Chip Carrier	73M2901C/5V-32IH	73M2901C-32IH
73M2901C 44-Pin Thin Quad Flat Pack	73M2901C/5V-IGT	73M2901C-IGT

DATA SHEET

TDK Semiconductor Corp., 2642 Michelle Dr., Tustin, CA 92780, (714) 508-8800, FAX (714) 508-8877