TDK SEMICONDUCTOR CORP.

78P2351
Single Channel
OC-3/ STM1-E/ E4 LIU

PRELIMINARY DATASHEET

FEBRUARY 2004

DESCRIPTION

The 78P2351 is TDK's second generation Line Interface Unit (LIU) for 155 Mbit/s SDH/SONET (OC-3, STS-3, or STM-1) and 140Mbit/s PDH (E4) applications. The device is a single chip solution that includes an integrated CDR in the transmit path for flexible NRZ to CMI conversion. The device can interface to 75Ω coaxial cable using CMI coding or directly to a fiber optics module using NRZ coding. The 78P2351 is compliant with all respective ANSI, ITU-T, and Telcordia standards for jitter tolerance, generation, and transfer.

APPLICATIONS

- Central Office Interconnects
- DSLAMs
- Add Drop Multiplexers (ADMs)
- PDH/SDH test equipment
- Multi Service Switches

FEATURES

- G.703 compliant, adjustable cable driver for 139.264 Mbps or 155.52 Mbps CMI-coded coax transmission
- Integrated adaptive CMI equalizer and CDR in receive path handles over 15dB of cable loss
- Serial, LVPECL-compatible system interface with integrated CDR in transmit path for flexible NRZ to CMI conversion.
- 4-bit parallel CMOS system interface with master/slave Tx clock modes.
- Selectable LVPECL compatible NRZ line interface for 155.52 Mbps optical transmission.
- Configurable via HW control pins or 4-wire serial port interface
- Optional fixed backplane equalizer compensates for up to 1.5m of trace
- Compliant with ANSI T1.105.03-1994; ITU-T G.751, G.813, G.823, G.825, G.958; and Telcordia GR-253-CORE for jitter performance.
- Loss of Lock (LOL) and standards compliant Loss of Signal (LOS) detection.
- Receive Monitor Mode handles up to 20dB of flat loss (at max 6dB cable loss)
- Operates from a single 3.3V supply
- 100-pin JEDEC LQFP

BLOCK DIAGRAM

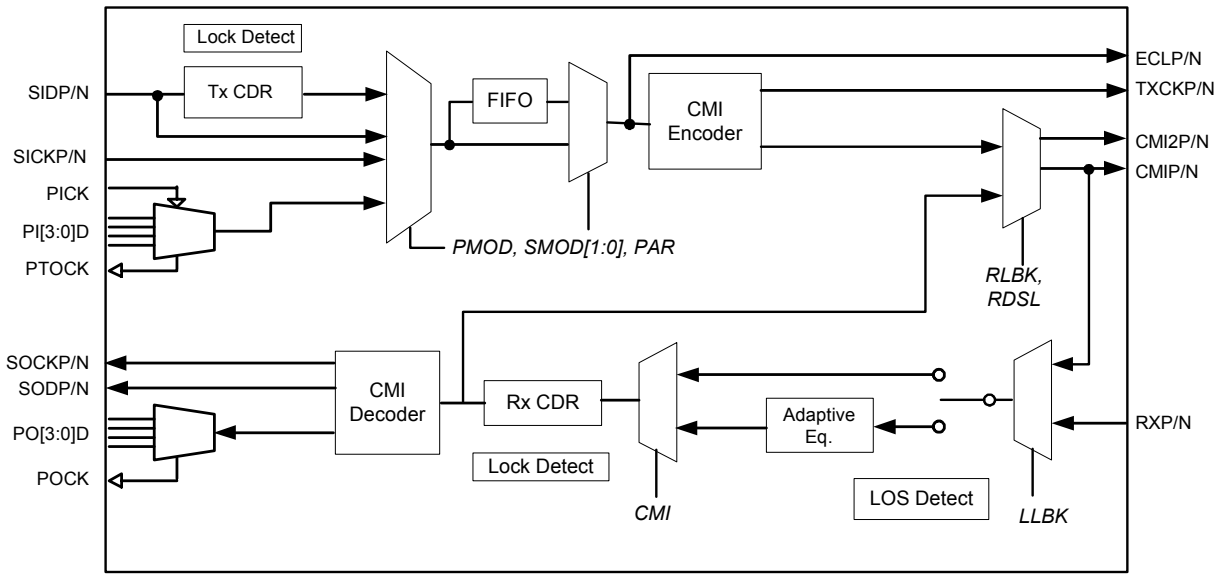


TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

FUNCTIONAL DESCRIPTION

The 78P2351 contains all the necessary transmit and receive circuitry for connection between 139.264Mbit/s and 155.52Mbit/s line interfaces and the digital universe. The chip is controllable through pins or serial port register settings.

In hardware mode (pin control) the SPSL pin must be low.

In software mode (SPSL pin high), control pins are disabled and the 78P2351 must be configured via the 4-wire serial port.

MODE SELECTION

The SDO_E4 pin or E4 register bit determines which rate the device operates in according to the table below. This control combined with CKSL also selects the reference frequency.

Rate	SDO_E4 pin	E4 bit
E4	High	1
STM-1, STS-3, OC-3	Low	0

The SEN_CMI pin or CMI register bit selects one of two media for reception and transmission: coaxial cable in CMI coding or optical fiber in NRZ coding.

Media (coding)	SEN_CMI pin	CMI bit
75 ohm Coax (CMI)	High	1
Fiber (NRZ)	Low	0

The SDI_PAR pin or PAR register bit selects the interface to the framer to be four-bit parallel CMOS or serial LVPECL. For each interface there are different transmit timing modes. See TRANSMITTER OPERATION section for more info.

REFERENCE CLOCK

The 78P2351 requires a reference clock supplied to the CKREFP/N pins. For reference frequencies of 77.76MHz or lower, the device accepts a single ended CMOS clock at CKREFP. For reference frequencies of 139.264/155.52MHz, the device accepts a differential LVPECL clock input at CKREFP/N. The frequency of this reference input is controlled by the rate selection and the CKSL control pin or register bit.

CKSL pin	Reference Frequency	
	SDO_E4 low	SDO_E4 high
Low	19.44MHz	17.408MHz
Float	77.76MHz	N/A
High	155.52MHz	139.264MHz
CKSL[1:0] bits	**E4 bit = 0**	**E4 bit = 1**
0 0	19.44MHz	17.408MHz
1 0	77.76MHz	N/A
1 1	155.52MHz	139.264MHz

RECEIVER OPERATION

The receiver accepts serial data, at 155.52Mbit/s or 139.264Mbit/s from the RXP/N inputs. In CMI mode, the CMI-coded inputs come from a coaxial cable that is transformer-coupled to the chip. In NRZ (optical) mode, the input pins receive NRZ LVPECL level signals from an O/E converter.

The CMI signal first enters an AGC and a high performance adaptive equalizer designed to overcome inter-symbol interference caused by long cable lengths. The variable gain differential amplifier automatically controls the gain to maintain a constant voltage level output regardless of the input voltage level. In ECL (NRZ) mode, the input signals bypass the adaptive equalizer.

The outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a digital PLL, which uses a reference frequency derived from the clock applied to the CKREFP/N pins.

In serial mode, the clock and data are transmitted through the LVPECL drivers. In parallel mode, the data is converted into four bit parallel segments before being transmitted through the CMOS drivers.

Receiver Monitor Mode

In CMI mode, the SCK_MON pin or MON register bit puts the receiver in monitor mode and adds approximately 20dB of flat gain to the receive signal before equalization. Rx Monitor Mode can handle 20dB of flat loss typical of monitoring points with up to 6dB of cable loss. Note that Loss of Signal detection is disabled during Rx Monitor Mode.

Loss of Signal

The 78P2351 includes an ITU-T G.775/G.783 compliant Loss of Signal (LOS) detector. When the received signal is less than approximately 18dB below nominal for 80 UI, the LOS pin is asserted. The LOS signal is cleared when the received signal is greater than approximately 17dB below nominal for 80 UI. During LOS conditions, the receive data outputs are squelched and held at logic '0'.

Note: Loss of Signal detection is disabled during Local Loopback and Receive Monitor Mode.

In ECL mode, the LOS signal will be asserted when there are no transitions for longer than 2.3µs. The signal is cleared when there are more than 4 transitions in 32 UI.

Loss of Lock

The 78P2351 will declare a loss of lock condition when the recovered clock frequency differs from the reference clock by more than ±100ppm in an interval greater than 420µs. This condition is cleared when the frequencies are less than ±100ppm off for more than 500µs.

FUNCTIONAL DESCRIPTION (continued)

TRANSMITTER OPERATION

The transmitter section generates an analog signal for transmission through either a transformer onto the coaxial cable using CMI coding or directly to a fiber optics module using NRZ coding.

The 78P2351 provides a flexible system interface for compatibility with most off-the-shelf framers and custom ASICs. The device supports a 4-bit parallel interface in either slave or master clocking modes and a number of serial NRZ timing modes.

Each of the serial NRZ transmit timing modes can be configured in HW mode or SW mode as shown in the table below.

Serial Mode	HW Control Pins		SW Control Bits	
	SDI_PAR	CKMODE	PAR	SMOD[1:0]
Synchronous clock + data	Low	Low	0	0 0
Synchronous data only	Low	Floating	0	1 0
Plesiochronous data only	Low	High	0	0 1
Loop-timig	n/a	n/a	X	11

Synchronous Serial Modes

In Figure 1, serial NRZ transmit data is input to the SIDP/N pins at LVPECL levels. By default, the data is latched in on the rising edge of SICKP. A clock decoupling FIFO is provided to decouple the on chip and off chip clocks. The SICKP/N clock provided by the framer/mapper IC must be source synchronous with the internal reference transmit clock if the FIFO is to be used.

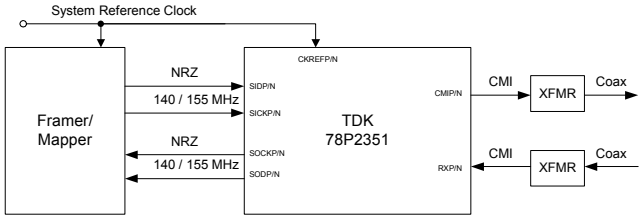


Figure 1: Synchronous; clock and data available (Tx CDR bypassed, FIFO enabled)

If no serial transmit clock is available, as in Figure 2, the 78P2351 can recover a clock from the serial NRZ data input and pass the data through the FIFO. In this mode, the NRZ transmit data should be source synchronous with the reference clock applied at CKREFP/N. The transmitter also includes a Loss of Lock indicator (TXLOL) that can be used to trigger an interrupt. Note that the FIFO is automatically re-centered when the TXLOL register bit transitions from high to low.

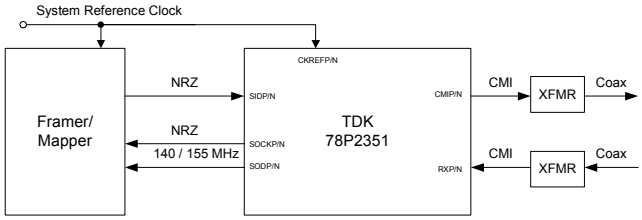


Figure 2: Synchronous; data only (Tx CDR enabled, FIFO enabled)

Since the reference clock and transmit clock/data go through different delay paths, it is inevitable that the phase relationship between the two clocks can vary in a bounded manner due to the fact that the absolute delays in the two paths can vary over time. The FIFO allows long-term clock phase drift, not exceeding +/- 25.6ns, to be handled without transmit error. If the clock wander exceeds the specified limits, the FIFO will over or under flow, and the FERR register signal will be asserted. This signal can be used to trigger an interrupt. This interrupt event is cleared when an FRST pulse is applied, and the FIFO is re-centered.

> **Note**: External remote loopbacks (i.e. loopback within framer) are not possible in synchronous operation (FIFO enabled) unless the reference clock is synchronous with the recovered receive clock (loop-timing).

Plesiochronous Serial Mode

Figure 3 represents the condition where no serial transmit clock is available and the data is not source synchronous to the reference clock input. In this mode, the 78P2351 will recover a clock from the serial plesiochronous data and bypass the FIFO.

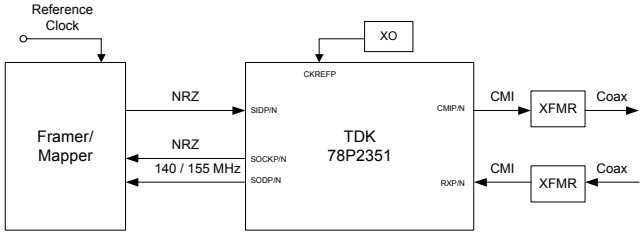


Figure 3: Plesiochronous; data only (Tx CDR enabled, FIFO bypassed)

FUNCTIONAL DESCRIPTION (continued)

Parallel Modes

In parallel modes, 4-bit CMOS data segments are input to the chip with a 34.816MHz (E4) or 38.88MHz (STM1) clock. These inputs are passed to the 4x8 decoupling FIFO and then to a serializer for transmission. For maximum compatibility, the 78P2351 can operate in both slave and master clock modes as shown in Figures 4 and 5 respectively. A loop-timing mode is also available to allow external remote loopbacks (i.e. line loopback in framer).

Parallel Mode	HW Control Pins		SW Control Bits	
	SDI_PAR	CKMODE	PAR	PMODE
Slave	High	Low	1	0
Slave + *Loop-timing	High	Float	1	1
Master	High	High	1	1

*Loop-timing in software mode requires SMOD[1:0]=11

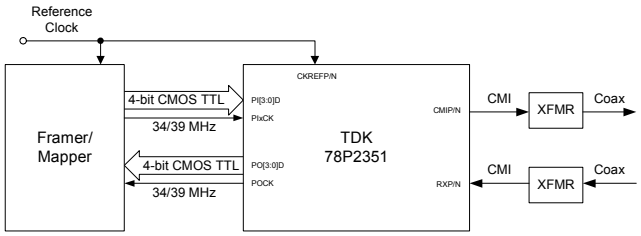


Figure 4: Slave Parallel Mode

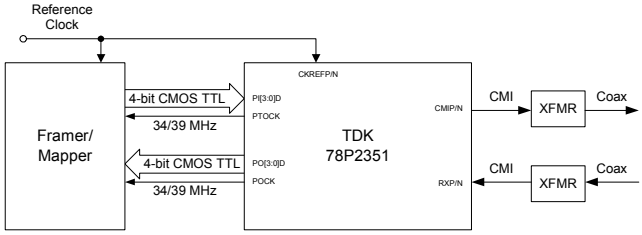


Figure 5: Master Parallel Mode

Transmit Driver

In CMI (electrical) mode, the CMIP/N pins connect the chip to 75Ω coaxial cable through a transformer and termination resistors. The transmitter converts the data to CMI coding and shapes an analog signal to meet the appropriate ITU-T G.703 template. The CMI outputs are tri-stated during transmit disable and transmit power-down for redundancy applications.

When the CMI pin is low, the chip is in NRZ (optical) mode. The output data signal from the ECLP/N pins have LVPECL levels and interface directly to a fiber module. The CMI driver, encoder and decoder are disabled in NRZ (optical) mode.

Pulse Amplitude Adjustment

Controls for adjusting the transmit pulse amplitude are provided in both hardware and software modes. Amplitude boosts of 5% and 10% can be enabled by the TXOUT0 pin or BST[1:0] register bits as follows:

TXOUT0 pin	BST[1:0] bits	Amplitude
Low	0 0	Normal
Float	0 1	5% boost
High	1 1	10% boost

Transmit Monitor Mode

An optional redundant transmit output is available in CMI mode for transmit monitoring. These outputs (CMI2P/N) are activated when the RCSL pin or RCSL register bit is activated.

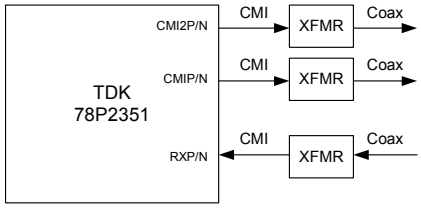


Figure 6: Transmit Monitor Output

Clock Synthesizer

The transmit clock synthesizer is a low-jitter PLL that generates a 278.528/311.04 MHz clock for the CMI encoder. A synthesized 139.264/155.52 MHz reference clock is also used in both the receive and transmit sides for clock and data recovery.

The 2x line rate clock is also available at the TXCKxP/N pins for downstream synchronization or interfacing to equipment lacking integrated clock recovery.

Transmit Backplane Equalizer

An optional fixed equalizer is integrated in the transmit path for architectures that use LIUs on active interface cards. The fixed equalizer can compensate for up to 1.5m of trace and can be enabled by the TXOUT1 pin or TXEQ bit as follows:

TXOUT1 pin	TXEQ bit	Tx Equalizer
Low	1	Enabled
Float	0	Disabled

Transmit Loss of Lock

In serial modes using the integrated CDR, the 78P2351 will declare a loss of lock condition when the recovered transmit clock frequency differs from the reference clock by more than ±100ppm in an interval greater than 420µs. This condition is cleared when the frequencies are less than ±100ppm off for more than 500µs.

FUNCTIONAL DESCRIPTION (continued)

POWER-DOWN FUNCTION

Power-down control is provided to allow the 78P2351 to be shut off. Transmit and receive power-down can be set independently through SW control. Global power-down is achieved by powering down both the transmitter and receiver.

Note: the serial interface and configuration registers are not affected by power-down.

The transmitter can also be powered down using the TXPD control pin. The CMI outputs are tri-stated during transmit power-down for redundancy applications. The TXPD pin is active in both hardware and software modes.

LOOPBACK MODES

In SW mode, LLBK and RLBK bits are provided to activate the local and remote loopback modes respectively. In HW mode, the LPBK pin can be used to activate local and remote loopback modes as shown below.

LPBK pin	Loopback Mode
Low	Normal operation
Float	Remote (digital) Loopback: Recovered receive clock and data looped back to transmitter
High	Local (analog) Loopback: Transmit clock and data looped back to receiver

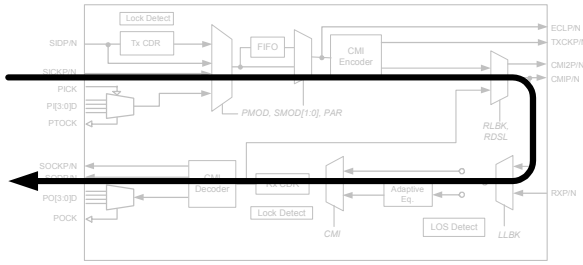


Figure 7: Local (Analog) Loopback

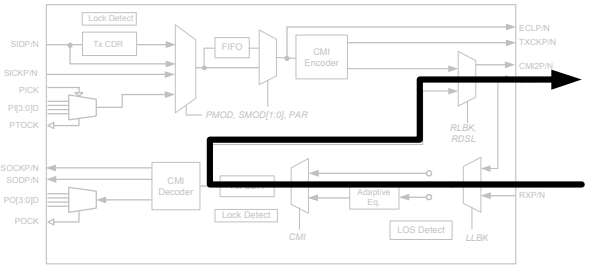


Figure 8: Remote (Digital) Loopback

INTERNAL POWER-ON RESET

Power-On Reset (POR) function is provided on chip. Roughly 50us after Vcc reaches 2.4V at power up, a reset pulse is internally generated. This resets all registers to their default values as well as all state machines within the transceiver to known initial values. The reset signal is also brought out to the PORB pin. The PORB pin is a special function pin that allows for the following:

- Override the internal POR signal by driving in an external active low reset signal;
- Use the POR signal to drive other IC's power-on reset;
- Add external capacitor to slow down the release of power-on reset (approximately 8μs per nF added).

SERIAL CONTROL INTERFACE

The serial port controlled register allows a generic controller to interface with the 78P2351. It is used for mode settings, diagnostics and test, retrieval of status and performance information, and for on-chip trimming. The SPSL pin must be high in order to use the serial port.

The serial interface consists of four pins: Serial Port Enable (SEN_CMI), Serial Clock (SCK_MON), Serial Data In (SDI_PAR), and Serial Data Out (SDO_E4). The SEN_CMI pin initiates the read and write operations. It can also be used to select a particular device allowing SCK_MON, SDI_PAR and SDO_E4 to be bussed together. SCK_MON is the clock input that times the data on SDI_PAR and SDO_E4. Data on SDI_PAR is latched in on the rising-edge of SCK_MON, and data on SDO_E4 is clocked out using the falling edge of SCK_MON.

SDI_PAR is used to insert mode, address, and register data into the chip. Address and Data information are input least significant bit (LSB) first. The mode and address bit assignment and register table are shown in the following section.

SDO_E4 is a tristate capable output. It is used to output register data during a read operation. SDO_E4 output is normally high impedance, and is enabled only during the duration when register data is being clocked out. Read data is clocked out least significant bit (LSB) first.

If SDI_PAR coming out of the micro-controller chip is also tristate capable, SDI_PAR and SDO_E4 can be connected together to simplify connections.

PROGRAMMABLE INTERRUPTS

In addition to the receiver LOS and LOL status pins, the 78P2351 provides a programmable interrupt for each transmitter. In HW control mode, the default functions of the Tx interrupt is a transmit Loss of Lock (TXLOL) or FIFO error (FERR).

REGISTER DESCRIPTION

REGISTER ADDRESSING

Address Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Port Address				Sub-Address			Read/ Write
Assignment	PA[3]	PA[2]	PA[1]	PA[0]	SA[2]	SA[1]	SA[0]	R/W*

REGISTER TABLE

a) PA[3:0] = 0 : Global Registers

Sub Addr	Reg. Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	MSCR (R/W)	Master Control	E4 <0>	-- <0>	PAR <0>	CKSL[1] <X>	CKSL[0] <X>	-- <X>	-- <X>	SRST <0>
1	INTC (R/W)	Interrupt Control	INPOL <0>	-- <0>	-- <1>	-- <0>	-- <0>	-- <X>	MTLOL <1>	MFERR <1>
2	IOCR (R/W)	I/O Control	-- <X>	-- <X>	-- <X>	-- <X>	-- <X>	-- <X>	-- <X>	RCSL <0>

b) PA[3:0] = 1 : Port-Specific Registers

Sub Addr	Reg. Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	MDCR (R/W)	Mode Control	PDTX <0>	PDRX <0>	PMODE <X>	SMOD[1] <X>	SMOD[0] <X>	MON <0>	-- <0>	-- <1>
1	SGCR (R/W)	Signal Control	-- <0>	-- <0>	LOLOR <0>	RLBK <0>	LLBK <0>	RCLKP <0>	TCLKP <0>	FRST <0>
2	ACR1 (R/W)	Advanced Tx Control 1	-- <0>	-- <0>	-- <0>	-- <0>	-- <0>	-- <0>	TPK <0>	TXEQ <0>
3	ACR0 (R/W)	Advanced Tx Control 0	-- <1>	-- <0>	-- <1>	-- <0>	-- <1>	BST[1] <0>	BST[0] <0>	-- <0>
4	MCR2 (R/W)	Mode Control 2	CMI <1>	-- <X>	-- <X>	-- <0>	-- <0>	-- <0>	-- <0>	-- <0>
5	STAT (R/C)	Status Monitor	-- <X>	-- <X>	-- <X>	RXLOS <X>	RXLOL <X>	-- <X>	TXLOL <X>	FERR <X>
6-7	--	Reserved	--	--	--	--	--	--	--	--

REGISTER DESCRIPTION (continued)

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
R/O	Read only	R/W	Read or Write
R/C	Read and Clear		

GLOBAL REGISTERS

ADDRESS 0-0: MASTER CONTROL REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	E4	R/W	0	**Line Rate Selection**: Selects the line rate of all channels as well as the input clock frequency at the CKREFP/N pins. 0: OC-3, STS-3, STM-1 (155.52MHz) 1: E4 (139.264MHz)
6	--	R/W	0	Unused
5	PAR	R/W	0	**Serial/Parallel Interface Selection**: Selects the interface to the framer. 0: Serial LVPECL 1: 4-bit Parallel CMOS
4:3	CKSL [1:0]	R/W	XX	**Reference Clock Frequency Selection**: Selects the reference clock frequency input at CKREFP/N pins. 11: 155.52MHz / 139.264MHz (differential) 10: 77.76MHz / NA (single-ended) 00: 19.44MHz / 17.408MHz (single-ended) Secondary values correspond to E4 frequencies. Default values depend on the CKSL pin selection upon reset or power up.
2:1	--	R/W	X0	Reserved.
0	SRST	R/W	0	**Register Soft-Reset**: When this bit is set, all registers are reset to their default values. This register bit is self-clearing.

REGISTER DESCRIPTION (continued)

ADDRESS 0-1: INTERRUPT CONTROL REGISTER

This register selects the events that would cause the interrupt pins to be activated. User may set as many bits as required.

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	INPOL	R/W	0	**Interrupt Pin Polarity Selection**: 0 : Interrupt output is active-low (default) 1 : Interrupt output is active-high
6:2	--	R/W	01000	Reserved
1	MTLOL	R/W	1	**TXLOL Error Mask** (active low): Gates the TXLOL register bit to the INTTXB interrupt pin. 0: Mask 1: Pass
0	MFERR	R/W	1	**FIERR Error Mask** (active low): Gates the respective FIERR register bit to the INTTXB interrupt pin. 0: Mask 1: Pass

ADDRESS 0-2: I/O CONTROL REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7:1	--	R/W	XXXXXXX	Unused
0	RCSL	R/W	0	**Redundant Channel Enable**: Enables transmit monitor outputs at CMI2P/N pins. 0: Disable 1: Enable

REGISTER DESCRIPTION (continued)

PORT-SPECIFIC REGISTERS

For PA[3:0] = 1 only. Accessing a register with port address greater than 1 constitutes an invalid command, and the read/write operation will be ignored.

ADDRESS 1-0: MODE CONTROL REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	PDTX	R/W	0	**Transmitter Power-Down**: 0 : Normal Operation 1 : Power-Down. CMI Transmit outputs are also tri-stated.
6	PDRX	R/W	0	**Receiver Power-Down**: 0 : Normal Operation 1 : Power-Down
5	PMODE	R/W	X	**Parallel Mode Interface Selection**: When PAR=1, (Master Control Regsiter: bit 5), PMODE selects the source of the transmit parallel clock, either taken from the framer externally or generated internally. Default value is determined by CKMODE pin setting upon power up or reset. 0: Slave Timing. PICK clock input to the transmitter 1: Master Timing. PTOCK clock output from the transmitter When PAR=0, PMODE is invalid and defaults to logic '1'
4	SMOD[1]	R/W	X	**Serial Mode Interface Selection**: When PAR=0 (Master Control Regsiter: bit 5), SMOD[1:0] configures the transmitter's system interface. Default values determined by CKMODE pin setting upon power up or reset. SMOD[1] SMOD[0] 0 0 Synchronous clock and data are passed through a FIFO. The CDR is bypassed. 1 0 Synchronous data is passed through the CDR and then through the FIFO. 0 1 Plesiochronous data is passed through the CDR to recover a clock. FIFO is bypassed because the data is not synchronous with the reference clock. 1 1 Loop Timing Mode Enable: The recovered receive clock is used as the reference for the transmitter. The transmit data is passed through the CDR, but the FIFO is bypassed. When PAR=1, setting SMOD[1:0] = 11 will enabled Loop Timing Mode. Default values are determined by CKMODE pin setting upon power up or reset as follows: CKMODE Low → SMOD[1:0] default = 00 (no effect) CKMODE Float → SMOD[1:0] default = 11 (loop-timing) CKMODE High → SMOD[1:0] default = 01 (no effect)
3	SMOD[0]	R/W	X	
2	MON	R/W	0	**Receive Monitor Mode Enable**: 0: Normal Operation 1: Adds 20dB of flat gain to the receive signal before equalization. NOTE: Monitor mode is only available in CMI mode.
1:0	--	R/W	00	Reserved

REGISTER DESCRIPTION (continued)

ADDRESS 1-1: SIGNAL CONTROL REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	TCMIINV	R/W	0	**Transmit CMI Inversion**: This bit will flip the polarity of the transmit CMI data outputs at CMIP/N. 0: Normal 1: Invert
6	RCMIINV	R/W	0	**Receive CMI Inversion**: This bit will flip the polarity of the receive CMI data inputs at RXP/N. 0: Normal 1: Invert
5	LOLOR	R/W	0	**Receive Loss of Lock/Signal Override:** When high, the RXLOL and RXLOS signals will always remain low. 0: Normal 1: Forces LOS and LOL outputs to be low and resets LOS counter
4	RLBK	R/W	0	**Loopback Selection**: RLBK LLBK 0 0 Normal operation 1 0 Remote Loopback Enable: Recovered receive data is looped back to the transmitter for retransmission. 0 1 Local Loopback Enable: The transmit data is looped back and used as the input to the receiver.
3	LLBK	R/W	0	
2	RCLKP	R/W	0	**Receive Clock Inversion Select**: This bit will invert the receive output clock. 0: Normal. Data clocked out on falling edge of receive clock. 1: Invert. Data clocked out on the rising edge of receive clock.
1	TCLKP	R/W	0	**Transmit Clock Inversion Select**: This bit will invert the transmit input system clock. 0: Normal. Data is clocked in on rising edge of the transmit clock. 1: Invert. Data is clocked in on the falling edge of the transmit clock.
0	FRST	R/W	0	**FIFO Reset**: 0: Normal operation 1: Reset FIFO pointers to default locations. NOTE: Transmit monitor port will also be affected by FRST

REGISTER DESCRIPTION (continued)

ADDRESS 1-2: ADVANCED TRANSMIT CONTROL REGISTER 1

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7:2	--	R/W	000000	Reserved.
1	TPK	R/W	0	**Transmit Driver Peaking Enable**: When high, adds a 2% peak to the beginning of a transition in the CMI line driver to compensate for low inductive backplanes. 0: Normal Operation 1: Add peaking
0	TXEQ	R/W	0	**Transmit Fixed Equalizer Enable**: When enabled, compensates for between 0.75m and 1.5m of FR4 trace to the serial LVPECL data inputs SIDP/N 0: Normal Operation 1: Enable equalizer

ADDRESS 1-3: ADVANCED TRANSMIT CONTROL REGISTER 0

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7:3	--	R/W	10101	Reserved.
2:1	BST[1:0]	R/W	00	**Transmit Driver Amplitude Boost**: Adds 5% or 10% of boost to the CMI output. 00 : Normal amplitude 01 : 5% boost 10 : Reserved 11 : 10% boost
0	--	R/W	0	Reserved.

ADDRESS 1-4: MODE CONTROL REGISTER 2

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	CMI	R/W	1	**Line Interface Mode Selection**: 0: Optical (LVPECL). CMI ENDEC and line driver are disabled. 1: Coaxial cable (CMI encoded). CMI ENDEC enabled. Optical (NRZ) interface disabled.
6:0	--	R/W	XX00000	Reserved.

REGISTER DESCRIPTION (continued)

ADDRESS 1-5: STATUS MONITOR REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7:5	--	R/C	XXX	Reserved.
4	RXLOS	R/C	X	**Loss of Signal Indication**: 0: Normal operation 1: Loss of signal condition detected
3	RXLOL	R/C	X	**Receive Loss of Lock Indication**: 0: Normal operation 1: Recovered receive clock frequency differs from the reference by more than +/- 100ppm.
2	--	R/C	X	Unused
1	TXLOL	R/C	X	**Transmit Loss of Lock Indication**: 0: Normal operation 1: Transmit CDR unlocked
0	FERR	R/C	X	**Transmit FIFO Error Indication**: This bit is set whenever the internal FERR signal is asserted, indicating that the FIFO is operating at its depth limit. It is reset to 0 when the FRST pin is asserted. 0: Normal operation 1: Transmit FIFO phase error

ADDRESS 1-6, 1-7: RESERVED

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7:0	RSVD	R/O	0	Reserved for test.

PIN DESCRIPTION

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
A	Analog Pin *(Tie unused pins to ground)*	PO	LVPECL-Compatible Differential Output *(Tie unused pins to supply or leave floating)*
CIS	CMOS Schmitt Trigger Input *(Tie unused pins to ground)*	CO	CMOS Digital Output *(Leave unused pins floating)*
CI	CMOS Digital Input *(Tie unused pins to ground)*	COZ	CMOS Tristate Digital Output *(Leave unused pins floating)*
CIU	CMOS Digital Input w/ Pull-up	OD	Open-drain Digital Output *(Leave unused pins floating)*
CID	CMOS Digital Input w/ Pull-down	S	Supply
CIT	3-State CMOS Digital Input	G	Ground
PI	LVPECL-Compatible Differential Input *(Tie unused pins to ground)*		

TRANSMITTER PINS

NAME	PIN	TYPE	DESCRIPTION
PI0D PI1D PI2D PI3D	24 25 26 27	CI	**Transmit Parallel Data Input**: Four-bit CMOS parallel (nibble) inputs. Data is latched in on the rising edge (default) of the transmit parallel clock and serialized with the MSB (PIx3D) transmitted first.
PICK	23	CIS	**Transmit Parallel Clock Input**: A 34.816 MHz (E4) or 38.88 MHz (STM1) CMOS clock input that must be source synchronous with the reference clock supplied at the CKREFP/N pins. Used in Slave Parallel Mode.
PTOCK	28	CO	**Transmit Parallel Clock Output**: A 34.816 MHz (E4) or 38.88 MHz (STM1) CMOS clock output that is intended to latch in synchronous parallel data. Active during reset. Used in Master Parallel Mode.
SIDP SIDN	8 9	PI	**Transmit Serial Data Input**: Differential NRZ data input. See *Transmitter Operation* section for more info on different clocking/timing modes.
SICKP SICKN	5 6	PI	**Transmit Serial Clock Input**: A 155.52MHz synchronous differential input clock used to clock in the serial NRZ data. By default, data is clocked in on the rising edge of SICKP.
CMIP CMIN	93 94	A	**Transmit Serial CMI Data Output**: A CMI encoded data signal conforming to the relevant ITU-T G.703 pulse templates when properly terminated and transformer coupled to 75ohm cable. Outputs are tri-stated when transmitter is disabled. Active, but undefined during reset.
CMI2P CMI2N	79 78	A	**Transmit Monitor Output**: Redundant CMI transmit driver enabled by RCSL control.
TXCKP TXCKN	96 97	PO	**Transmit Serial Clock Output**: An optional 2x line rate LVPECL clock output used to clock out the transmit CMI data. Used for diagnostics or far end re-timing. Active during reset.
ECLP ECLN	99 100	PO	**Transmit Serial LVPECL Data Output**: Transmit NRZ data used for interfacing with optical transceiver modules.

PIN DESCRIPTION (continued)

RECEIVER PINS

NAME	PIN	TYPE	DESCRIPTION
PO0D PO1D PO2D PO3D	41 40 37 36	CO	**Receive Data Parallel Output**: Recovered receive data deserialized into four-bit CMOS parallel (nibble) outputs. The MSB (PO3D) is received first. Active, but undefined during reset. Note: During Loss of Signal conditions, data outputs are held low.
POCK	33	CO	**Receive Parallel Clock Output**: A 34.816 MHz (E4) or 38.88 MHz (STM1) CMOS clock output generated by dividing down the recovered receive clock. By default, receive data is clocked out on the falling edge. Active during reset. Note: During Loss of Signal conditions, the clock automatically switches to a 34.816MHz (E4) or 38.88MHz (STM1) clock generated from the reference clock.
SODP SODN	20 21	PO	**Receive Serial Data Output**: Recovered receive serial NRZ data. Active, but undefined during reset. Note: During Loss of Signal conditions, data outputs are held low.
SOCKP SOCKN	18 19	PO	**Receive Serial Clock Output**: Recovered receive serial clock. By default, recovered serial NRZ data is clocked out the falling edge of SOxCKP. Active during reset. Note: During Loss of Signal conditions, the clock automatically switches to a divided down reference clock of 34.816MHz (E4) or 38.88MHz (STM1).
RXP RXN	90 91	A/ PI	**Receive Serial CMI or LVPECL Input**: The input signal is either differentially terminated and transformer coupled for CMI data or at LVPECL levels for NRZ data.

PIN DESCRIPTION (continued)

REFERENCE AND STATUS PINS

The LOS, LOL, and INTxXB pins are configurable at final test (default open-drain outputs). If CMOS level outputs are required, please refer to alternate ordering numbers at the end of the data sheet.

NAME	PIN	TYPE	DESCRIPTION
CKREFP CKREFN	83 82	PI/ CI	**Reference Clock Input**: A required reference clock input used for clock/data recovery and frequency synthesizer. Options include • 139.264 MHz (E4) or 155.52 MHz (STM1) differential LVPECL clock input at CKREFP/N • 17.408 MHz (E4), 19.44 MHz (STM1), or 77.78 MHz (STM1) single-ended CMOS clock input at CKREFP. Tie CKREFN to ground when unused.
LOS	61	OD/ CO	**Loss of Signal** (active-high): Standards compliant loss of signal indicator.
LOL	60	OD/ CO	**Loss of Lock** (active-high): This condition is met when the recovered clock frequency differs from the reference clock frequency by more than +/- 100ppm.
INTTXB	67	OD/ CO	**Transmitter Fault Interrupt Flag** (active low): When a transmitter error event occurs (as defined in the Interrupt Control Register Description), the INTTXB pin will change state to indicate an interrupt. The interrupt is cleared by a read to the STAT Register, an issue of a FRST FIFO reset pulse (if the FIERR signal caused the interrupt), or when the TXLOL register bit transitions from high to low. Note: The default interrupt condition is a loss of lock in the transmitter CDR.
INTRXB	52	OD/ CO	**Receiver Fault Interrupt Flag** (active-low): Reserved for future use.
PORB	64	A	**Power-On Reset** (active-low): See Power-On Reset description on use of this pin.

PIN DESCRIPTION (continued)

CONTROL PINS

NAME	PIN	TYPE	DESCRIPTION
FRST	59	CIT	**FIFO Phase-Initialization Control**: Should normally be floating or high. When asserted, the transmit FIFO pointers are reset to the respective "centered" states. Also resets the FIERR interrupt bit. De-assertion edge of FRST will resume FIFO operation. • Low: FRST assertion. • Float/High: Normal NOTE: Transmit Monitor port is also affected during a FIFO reset.
RCSL	14	CID	**Redundant Channel Selection**: Enables the redundant Transmit Monitor Output at pins CMI2P/N. • Low: Normal operation (CMIP/N active only) • High: Transmit Monitor Mode (CMIP/N and CMI2P/N active)
LPBK	15	CIT	**Loopback Selection**: • Low: Normal operation • Float: Remote Loopback Enable: Recovered receive data and clock are looped back to the transmitter for retransmission. • High: Local Loopback Enable: The serial transmit data is looped back and used as the input to the receiver.
CKMODE	13	CIT	**Clock Mode Selection**: In PARALLEL mode (SDI_PAR high): • Low: Parallel transmit clock is input to the 78P2351. • Float: Parallel transmit clock is input to the 78P2351. Loop-timing mode enabled. • High: Parallel transmit clock is output from the 78P2351 In SERIAL mode (SDI_PAR low): • Low: Reference clock is synchronous to transmit clock and data. Data is clocked in with SICKP/N and passed through a FIFO • Float: Reference clock is synchronous to transmit data. Clock is recovered with a CDR and data is passed through a FIFO • High: Reference clock is plesiochronous to transmit data. Clock is recovered with a CDR and the FIFO is bypassed

PIN DESCRIPTION (continued)

CONTROL PINS (continued)

NAME	PIN	TYPE	DESCRIPTION
TXOUT1	1	CIT	**Advanced Tx Control 1**: Low: Enables fixed LVPECL equalizer at the transmit inputs SIDP/N (for FR4 trace lengths up to 1.5m). Float: Normal operation High: Adds 2% positive peaking on leading edge (for bandwidth limiting components between LIU and coax connector)
TXOUT0	2	CIT	**Advanced Tx Control 0**: Low: Nominal amplitude Float: 5% amplitude boost High: 10% amplitude boost
TXPD	12	CID	**Transmitter Power Down**: When high, powers down the transmitter. The transmit monitor port, if enabled, is also powered down when TXPD is high.
SPSL	58	CID	**Serial Port Selection**: When high, chip is SW controlled through the serial port.
CKSL	62	CIT	**Reference Clock Frequency Selection**: Selects the reference frequency that is supplied at the CKREFP/N pins. Its level is read in only at power-up or on the rising edge of a reset signal at the PORB pin. • Low: 19.44MHz or 17.408MHz • Float: 77.76MHz • High: 155.52MHz or 139.264MHz

PIN DESCRIPTION (continued)

SERIAL-PORT PINS

NAME	PIN	TYPE	DESCRIPTION
SEN_CMI	72	CIT	[SPSL=1] **Serial-Port Enable**: High during read and write operations. Low disables the serial port. While SEN is low, SDO remains in high impedance state, and SDI and SCK activities are ignored. [SPSL=0] **Medium Select**: Low: ECL (NRZ) mode Float: CMI mode (input/output polarity inverted) High: CMI mode (normal input/output)
SCK_MON	73	CIS	[SPSL=1] **Serial Clock**: Controls the timing of SDI and SDO. [SPSL=0] **Receive Monitor Mode Enable**: When high, adds 20dB of flat gain to the incoming signal before equalization. NOTE: Rx Monitor mode is only available in CMI mode.
SDI_PAR	71	CI	[SPSL=1] **Serial Data Input**: Inputs mode and address information. Also inputs register data during a Write operation. Both address and data are input least significant bit first. [SPSL=0] **Data Width Select**: Selects 4 bit parallel (input high) or serial mode (input low)
SDO_E4	70	COZ/ CI	[SPSL=1] **Serial Data Output**: Outputs register information during a Read operation. Data is output least significant bit first [SPSL=0] **Rate Select**: Selects E4 operation (input high) or STM1/STS3 operation (input low)

POWER AND GROUND PINS

It is recommended that all supply pins be connected to a single power supply plane and all ground pins be connected to a single ground plane.

NAME	PIN	TYPE	DESCRIPTION
VCC	3, 10, 16, 56, 66, 69, 76, 80, 88, 92, 98	S	**Power Supply**
VDD	31, 35, 39, 43	S	**CMOS Driver Supply**
GND	4, 11, 17, 55, 63, 65, 68, 77, 84, 85, 86, 87, 89, 95	G	**Ground**
VSS	30, 34, 38, 42	G	**CMOS Driver Ground**

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond these limits may permanently damage the device.

PARAMETER	RATING
Supply Voltage (Vdd)	-0.5 to 4.0 VDC
Storage Temperature	-65 to 150 °C
Junction Temperature	-40 to 125 °C
Pin Voltage (CMIxP,CMIxN)	Vdd + 1.5 VDC
Pin Voltage (all other pins)	-0.3 to (Vdd+0.6) VDC
Pin Current	±100 mA

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

PARAMETER	RATING
DC Voltage Supply (Vdd)	3.15 to 3.45 VDC
Ambient Operating Temperature	-40 to 85°C

DC CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current (CMI) (including transmitter current through transformer)	Iddm	STM-1 mode; CMI mode; Max. cable length; Tx Monitor Enabled		190	212	mA
	Idd	STM-1 mode; CMI mode; Max. cable length; Tx Monitor Disabled		160	178	mA
Supply Current (NRZ)	Idde	STM-1 mode; NRZ (optical) mode;		145	162	mA
Receive-only Supply Current	Iddr	Transmitter disabled; STM-1 mode; CMI mode; Max. cable length;		92		mA
Power down Current	Iddq	PDTX=1, PDRX=1		7	10	mA

ELECTRICAL SPECIFICATIONS (continued)

ANALOG PINS CHARACTERISTICS:
The following table is provided for informative purpose only. Not tested in production.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
RXP and RXN Common-Mode Bias Voltage	Vblin	Ground Reference	1.9	2.1	2.6	V
RXP and RXN Differential Input Impedance	Rilin			20		kΩ
Analog Input/Output Capacitance	Cin			8		PF
PORB Input Impedance	--			5		kΩ

DIGITAL I/O CHARACTERISTICS:
Pins of type CI, CIU, CID:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	Vil				0.8	V
Input Voltage High	Vih		2.0			V
Input Current	Iil, Iih		-1	0	1	μA
Pull-up Resistance	Rpu	Type CIU only	53	70	113	kΩ
Pull-down Resistance	Rpd	Type CID only	43	58	118	kΩ
Input Capacitance	Cin			8		pF

Pins of type CIT:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	Vtil				0.4	V
Input Voltage High	Vtih		Vcc-0.8			V
Minimum impedance to be considered as “float” state	Rtiz		30			kΩ

Pins of type CIS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Low-to-High Threshold	Vt+		1.3		1.7	V
High-to-Low Threshold	Vt-		0.8		1.2	V
Input Current	Iil, Iih		-1		1	μA
Input Capacitance	Cin			8		pF

ELECTRICAL SPECIFICATIONS (continued)

Pins of type CO and COZ:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Iol = 8mA			0.4	V
Output Voltage High	Voh	Ioh = -8mA	2.4			V
Output Transition Time	Tt	C_L = 20pF			2	ns
Effective Source Impedance	Rscr			30		Ω
Tri-state Output Leakage Current	Iz	Type COZ only	-1		1	µA

Pins of type PO:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Signal Swing	Vpk		0.5	0.8	1.1	V
Common Mode Level	Vcm	Vdd referenced	-1.4	-1.2	-1.1	V
Effective Source Impedance	Reff			20		Ω
Rise Time	Tr	10-90%		0.8	1.2	ns
Fall Time	Tf	10-90%		0.8	1.2	ns

Pins of type PI:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Signal Swing	Vpki		0.3			V
Common Mode Level	Vcm	Vdd referenced	-1.6		-0.8	V

Pins of type OD

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Iol = 8mA			0.4	V
Pull-down Leakage Current	Ipd	Logic high output			1	nA
Pull-up Resistor	Rpu		4.7		10	kΩ

ELECTRICAL SPECIFICATIONS (continued)

SERIAL-PORT TIMING CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SDI to SCK setup time	tsu		4			ns
SDI to SCK hold time	th		4			ns
SCK to SDO propagation delay	tprop				10	ns
SCK frequency	SCK				20	MHz

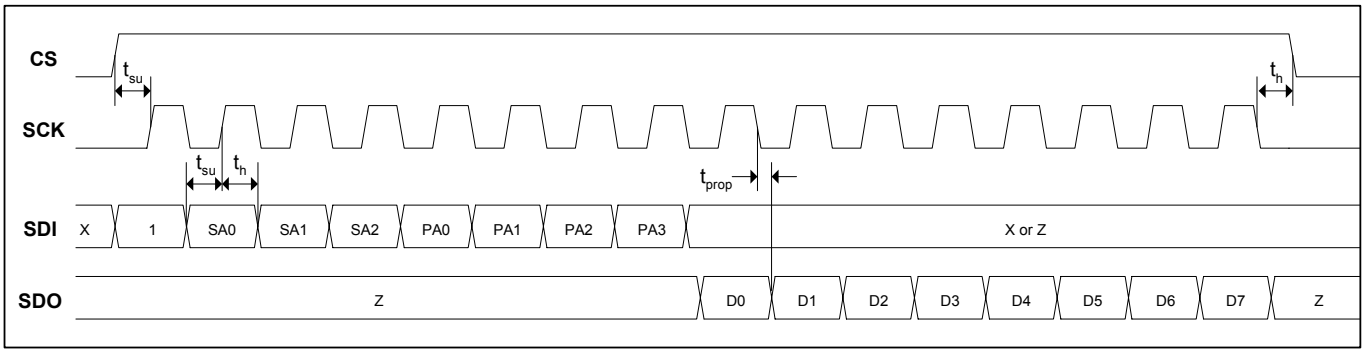


Figure 9: Read Operation

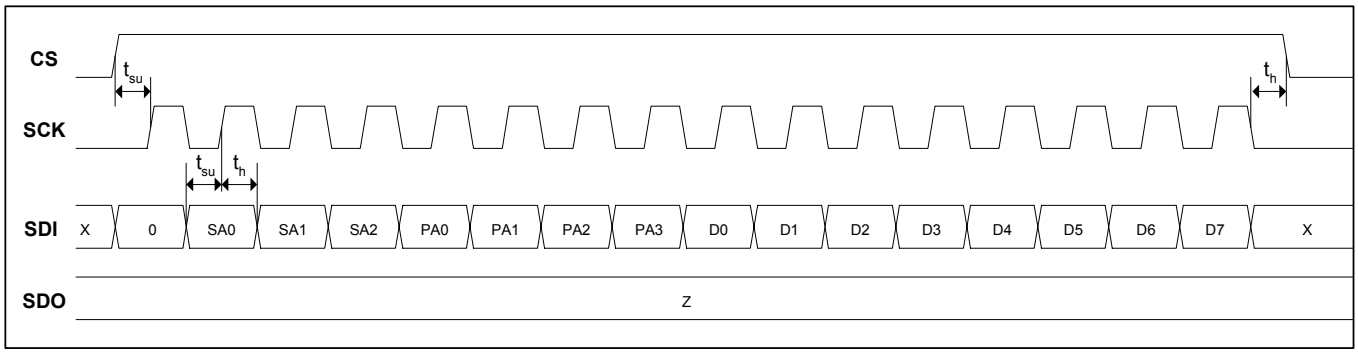


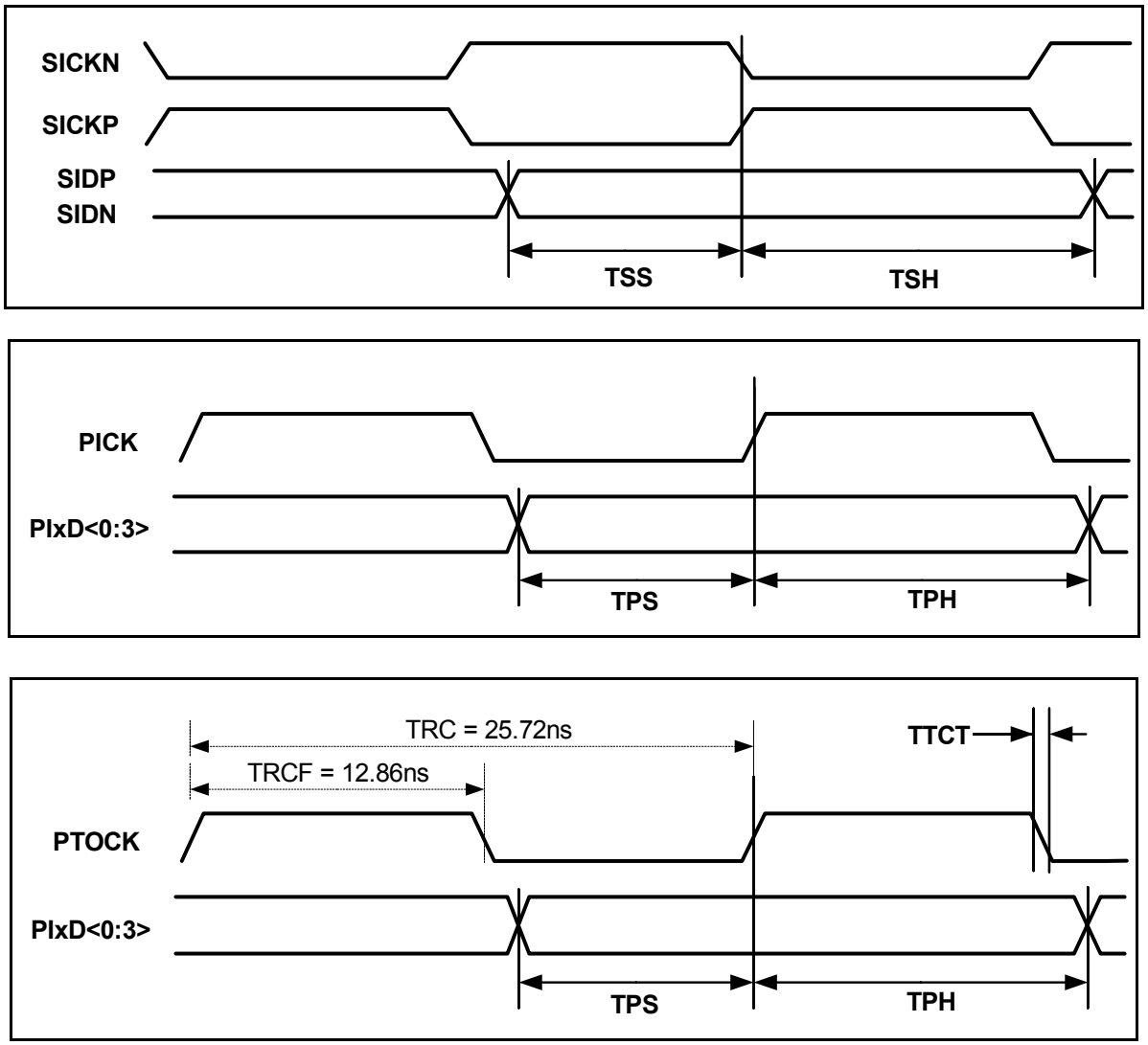
Figure 10: Write Operation

ELECTRICAL SPECIFICATIONS (continued)

TRANSMITTER TIMING CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Clock Duty Cycle	TTCF/TTC	PTOCK	40		60	%
Setup Time	TPS	Parallel mode	4			ns
Hold Time	TPH	Parallel mode	4			ns
Setup Time	TSS	Serial mode	2			ns
Hold Time	TSH	Serial mode	2			ns

TIMING DIAGRAM: Transmitter Waveforms



ELECTRICAL SPECIFICATIONS (continued)

REFERENCE CLOCK CHARACTERISTICS:

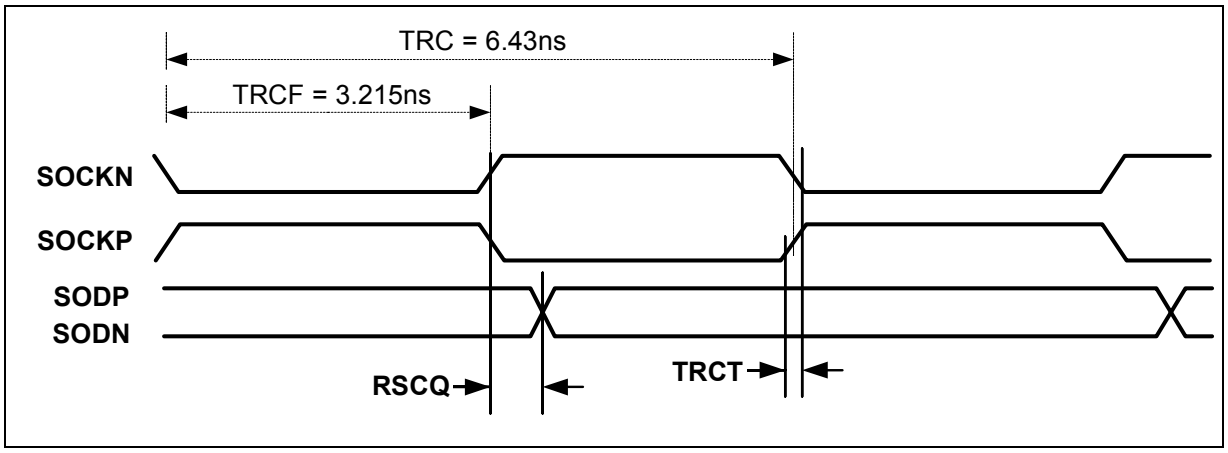
PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
CKREF Duty Cycle	--		40		60	%
CKREF Frequency Stability	--	Synchronous mode; E4	-15		+15	ppm
		Synchronous mode; STM1	-20		+20	
		Plesiochronous or Loop-timing mode. (see Note 1)	-75		+75	

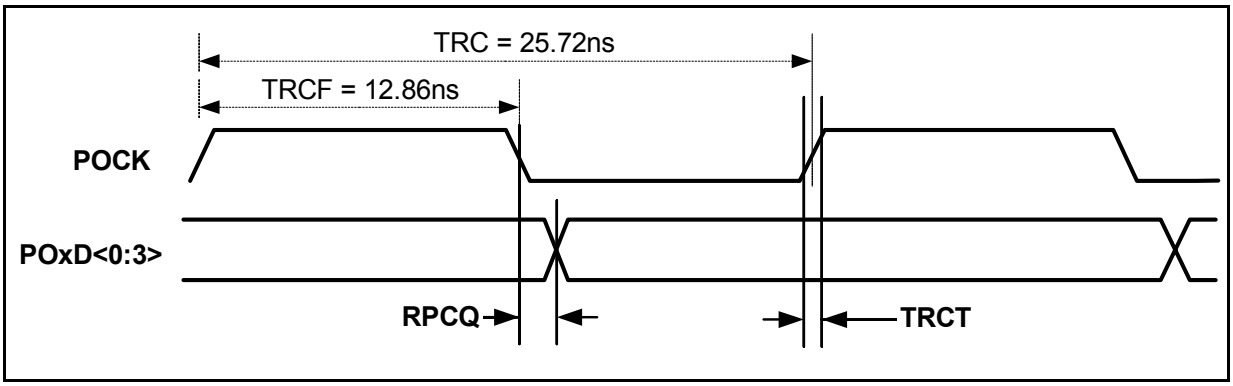
Note 1: In Plesiochronous mode, the transmit clock/data source (i.e. framer) must still be of +/-20ppm quality (+/-15ppm for E4) in order to meet the SONET/SDH requirements.

RECEIVER TIMING CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
RCLK Duty Cycle	TRCF/TRC		40		60	%
Clock to Q	RSCQ	Serial mode	0		1	ns
	RPCQ	Parallel mode	-1		2	

TIMING DIAGRAM: Receive Waveforms





ELECTRICAL SPECIFICATIONS (continued)

TRANSMITTER SPECIFICATIONS FOR CMI INTERFACE

Bit Rate: 139.264Mbit/s ± 15ppm or 155.52Mbits/s ± 20ppm
Code: Coded Mark Inversion (CMI)
Relevant Specification: ITU-T G.703

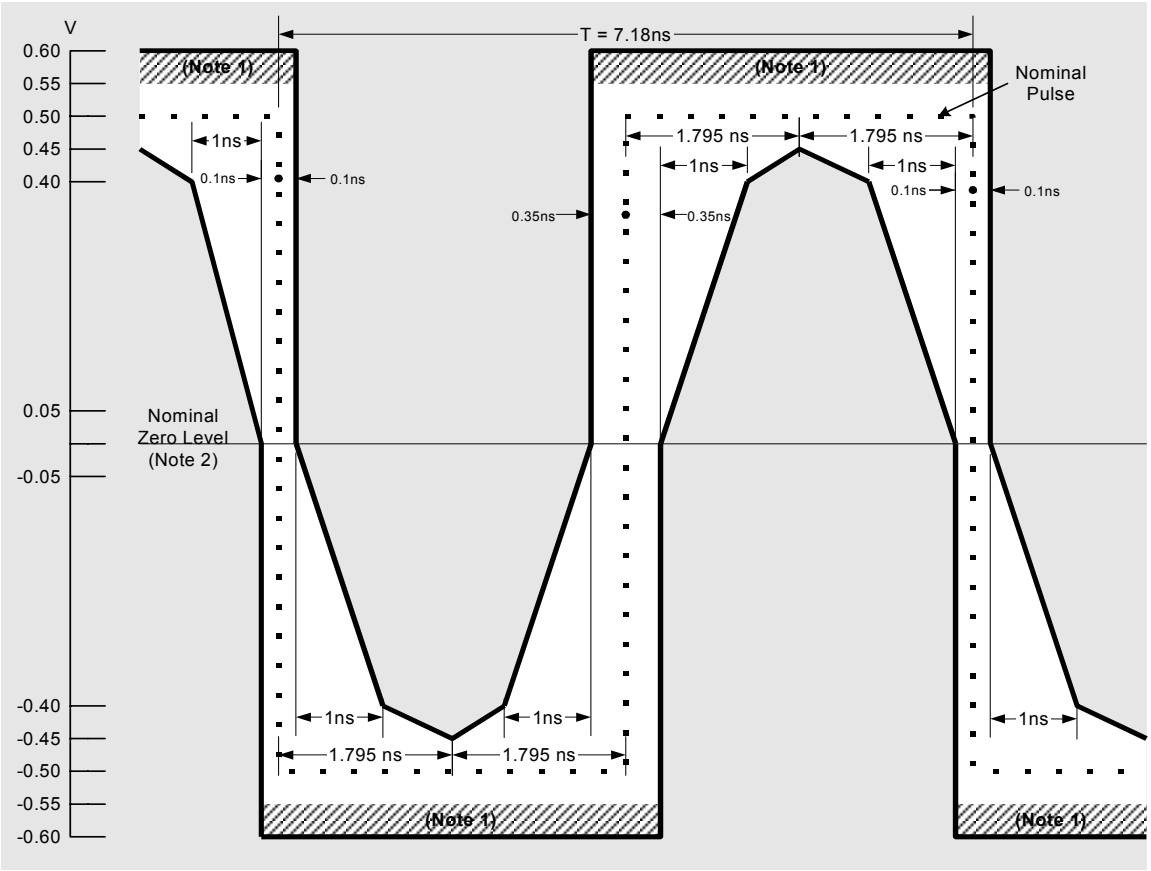
With the coaxial output port driving a 75Ω load, the output pulses conform to the templates in Figures 11, 12, 13 and 14. These specifications are tested during production test.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Peak-to-peak Output Voltage	Template, steady state	0.9		1.1	V
Rise/ Fall Time	10-90%			2	ns
Transition Timing Tolerance	Negative Transitions	-0.1		0.1	ns
	Positive Transitions at Interval Boundaries	-0.5		0.5	
	Positive Transitions at mid-interval	-0.35		0.35	
Transmit clock frequency stability (PICK or SICKP/N)	With respect to CKREF	0		0	ppm

The following specifications are not tested during production test. They are included for information only.
Note that the return loss depends on the board layout and the particular transformer used.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Impedance	Driver is open drain		1 8		MΩ pF
Return Loss	7MHz to 240MHz	15			dB

ELECTRICAL SPECIFICATIONS (continued)



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

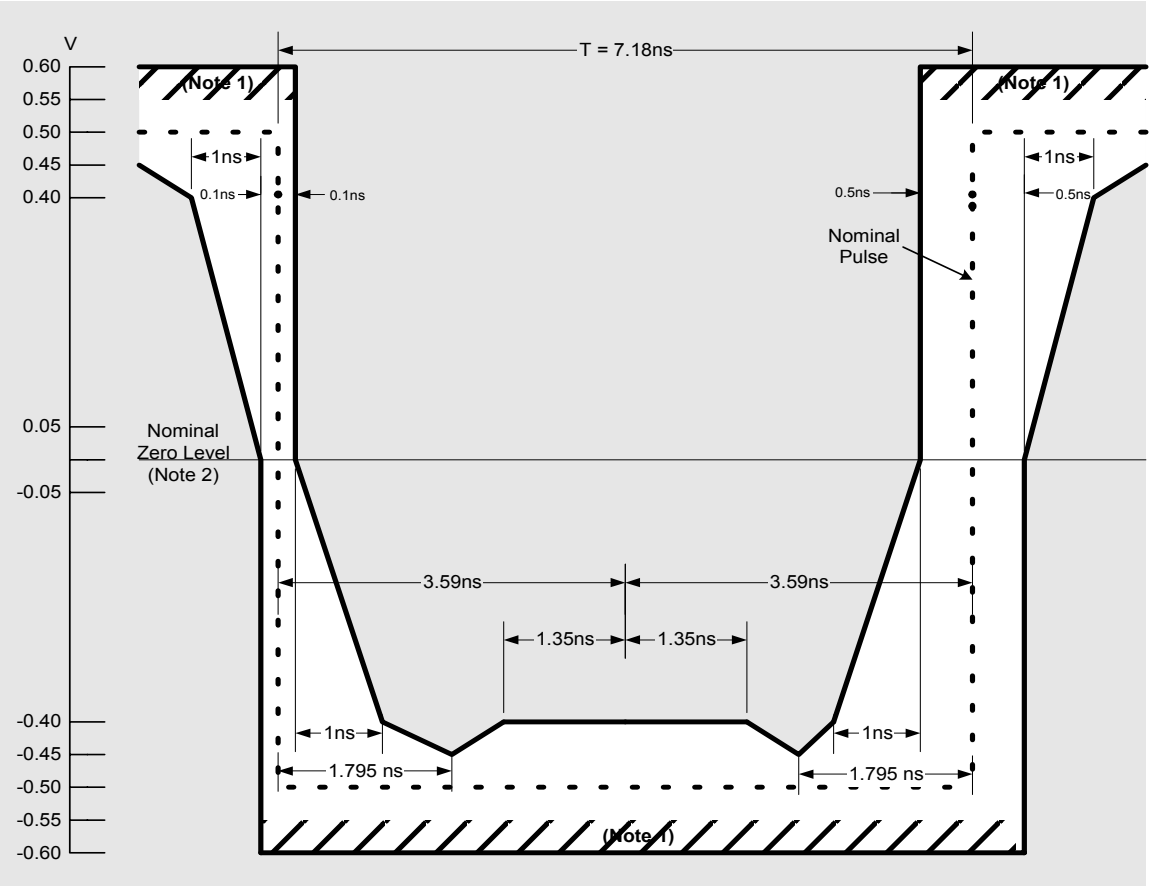
Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies with ±0.05V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

Figure 11 – Mask of a Pulse corresponding to a binary Zero in E4 mode

ELECTRICAL SPECIFICATIONS (continued)



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies with ±0.05V of the nominal zero level of the masks.

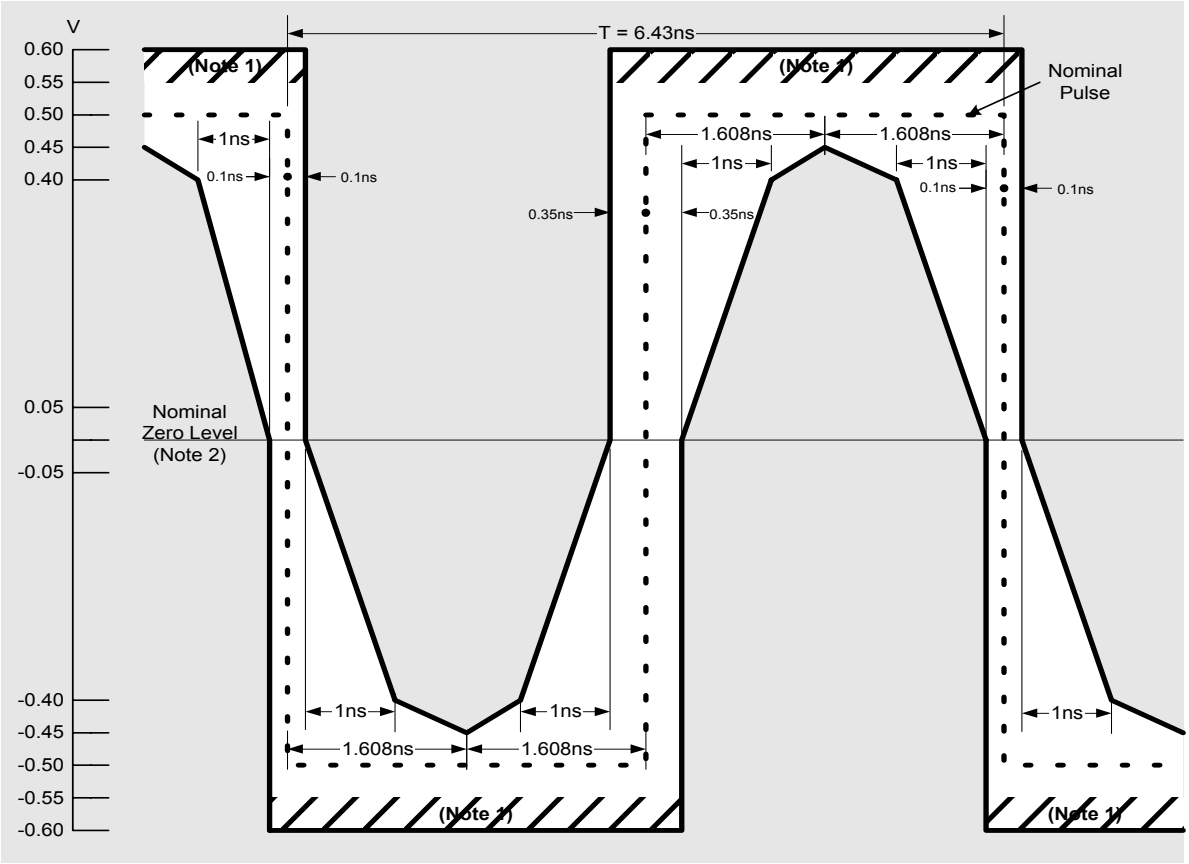
Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

Note 5 –The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ± 0.1ns and ±0.5ns respectively.

Figure 12 – Mask of a Pulse corresponding to a binary One in E4 mode.

ELECTRICAL SPECIFICATIONS (continued)



Note 1 – The maximum “steady state” amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

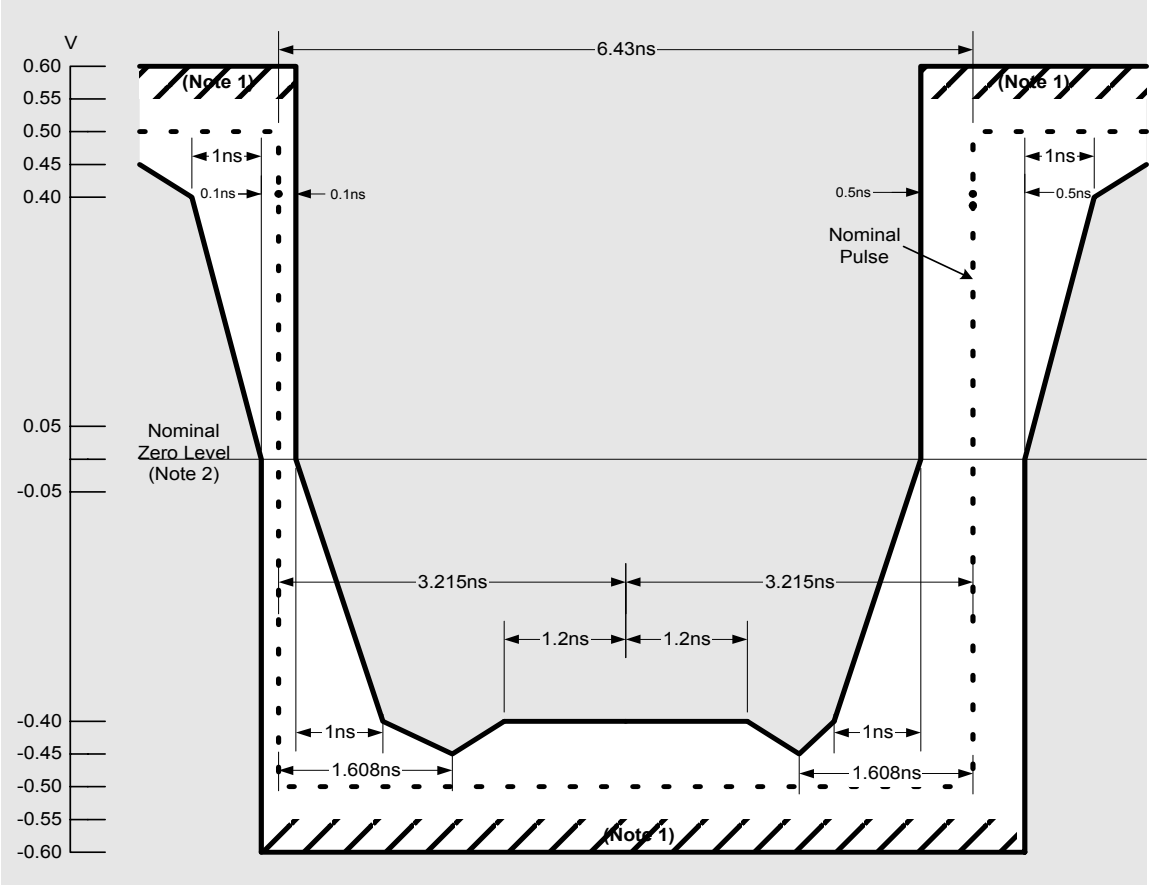
Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies with ±0.05V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

Figure 13 – Mask of a Pulse corresponding to a binary Zero in STM-1/STS-3 mode.

ELECTRICAL SPECIFICATIONS (continued)



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies with ±0.05V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

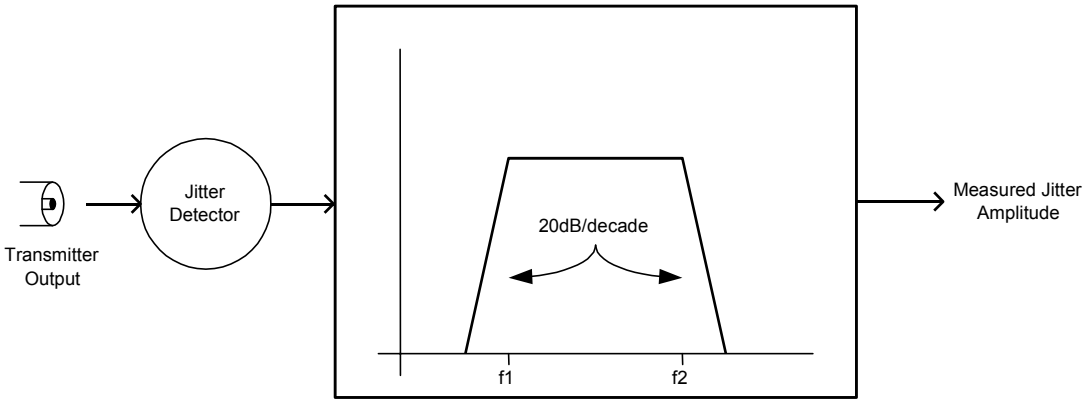
Note 5 –The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ± 0.1ns and ±0.5ns respectively.

Figure 14 – Mask of a Pulse corresponding to a binary One in STM-1/STS-3 mode

ELECTRICAL SPECIFICATIONS (continued)

TRANSMITTER OUTPUT JITTER

The transmit jitter specification ensures compliance with ITU-T G.813, G.823, G.825 and G.958; ANSI T1.102-1993 and T1.105.03-1994; and GR-253-CORE for all supported rates. Transmit output jitter is not tested during production test.



PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Transmitter Output Jitter	CMI Mode; 200 Hz to 3.5 MHz, measured with respect to CKREF for 60s			0.075	UIpp
	NRZ (optical) Mode; 12 kHz to 1.3 MHz, measured with respect to CKREF			0.01	UIrms

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER SPECIFICATIONS FOR CMI INTERFACE (Transformer-coupled)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Peak Differential Input Amplitude, RXP and RXN	CMI mode; MON=0; 12.7dB of cable loss	70		550	mVpk
Peak Differential Input Amplitude, RXP and RXN	CMI mode; MON=1; 20dB flat loss w/ 6dB of cable loss	25		80	mVpk
Flat-loss Tolerance	CMI mode; MON=0; All valid cable lengths.	-2		6	dB
Receive Clock Jitter	STM-1 mode; CMI mode; 12.7 dB cable loss a) Normal receive mode b) Remote loopback mode			 0.1 0.07	 UIpp UIpp
Latency			5	10	UI
PLL Lock Time			1	10	µs
Return Loss	7MHz to 240MHz	15			dB

The input signal is assumed compliant with ITU-T G.703 and can be attenuated by the dispersive loss of a cable. The minimum cable loss is 0dB and the maximum is –12dB at 70MHz.

The “Worst Case” line corresponds to the ITU-T G.703 recommendation. The “Typical” line corresponds to a typical installation referred to in ANSI T1.102-1993. The receiver is tested using the cable model. It is a lumped element approximation of the “Worst Case” line.

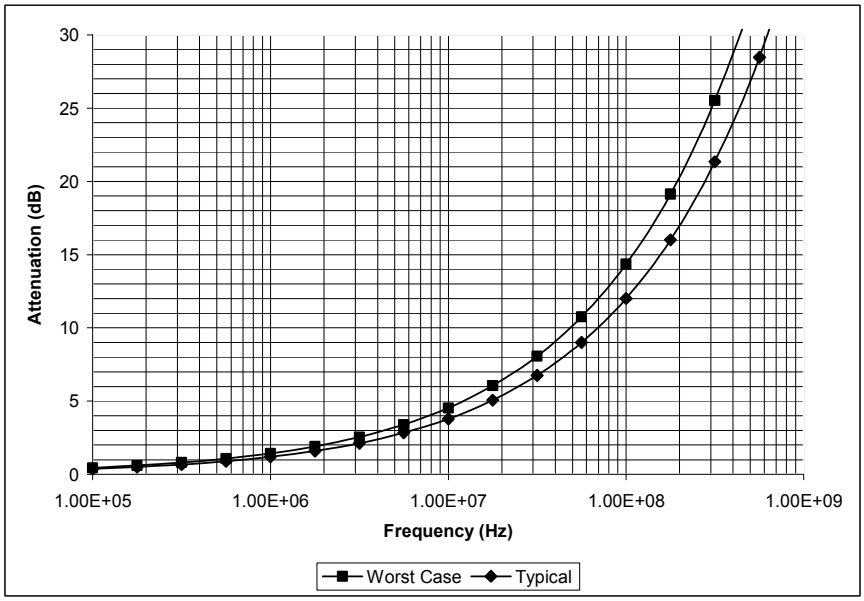


Figure 15: Typical and worst-case Cable attenuation

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER JITTER TOLERANCE

The 78P2351 is compliant with all relevant jitter tolerance specifications shown in Figures 16, 17. STS-3/OC-3 jitter tolerance specifications are in ANSI T1.105.03-1994 and Telcordia GR-253-CORE. STM-1 (optical) jitter tolerance specifications are in ITU-T G.813, G.825, and G.958. STM-1e (electrical) jitter tolerance specifications are in ITU-T G.825. E4 specifications are found in ITU-T G.823. Receive jitter tolerance is not tested during production test.

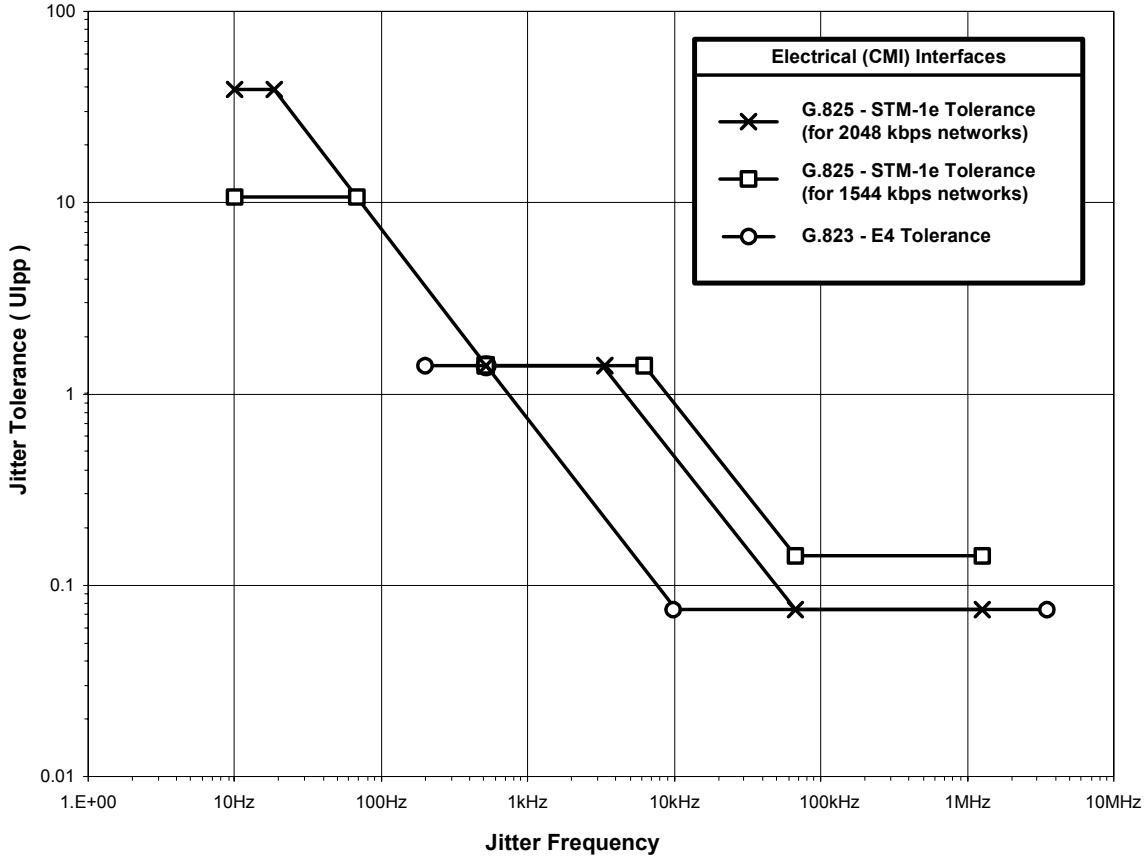


Figure 16: Jitter Tolerance - electrical (CMI) interfaces

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
E4 Jitter Tolerance	200Hz to 500Hz	1.5			UIpp
	500Hz to 10kHz		750 f-1		µs
	10kHz to 3.5MHz	0.075			UIpp
STM-1e Jitter Tolerance	10Hz to 19.3Hz	38.9			UIpp
	19.3Hz to 500Hz		750 f-1		µs
	500Hz to 6.5kHz	1.5			UIpp
	6.5kHz to 65kHz		9800 f-1		µs
	65kHz to 1.3MHz	0.15			UIpp

ELECTRICAL SPECIFICATIONS (continued)

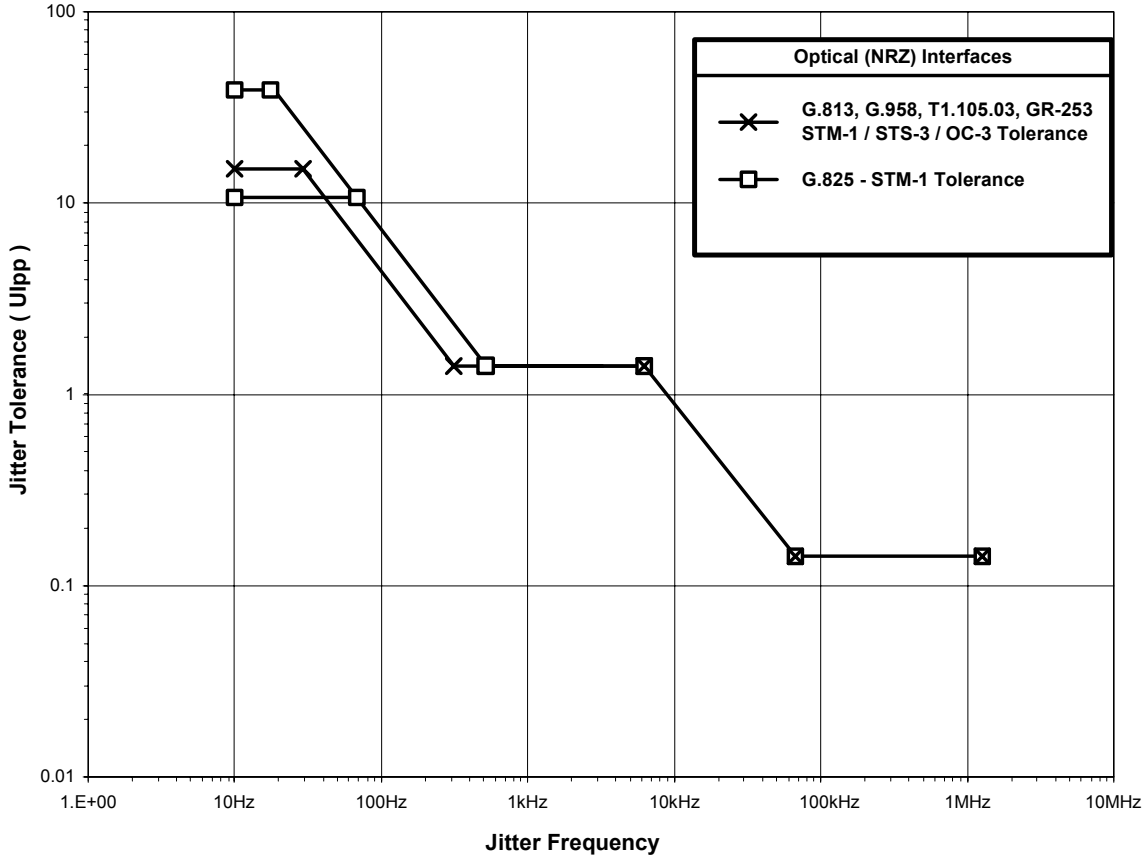


Figure 17: Jitter Tolerance - optical (NRZ) interfaces

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
OC-3/STS-3/STM-1 (optical) Jitter Tolerance	10Hz to 19.3Hz	38.9			UIpp
	19.3Hz to 68.7Hz		750 f-1		µs
	68.7Hz to 6.5kHz	1.5			UIpp
	6.5kHz to 65kHz		9800 f-1		µs
	65kHz to 1.3MHz	0.15			UIpp

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER JITTER TRANSFER FUNCTION

The receiver clock recovery loop filter characteristics such that the receiver has the following transfer function. The corner frequency of the PLL is approximately 120 kHz. Receiver jitter transfer function is not tested during production test.

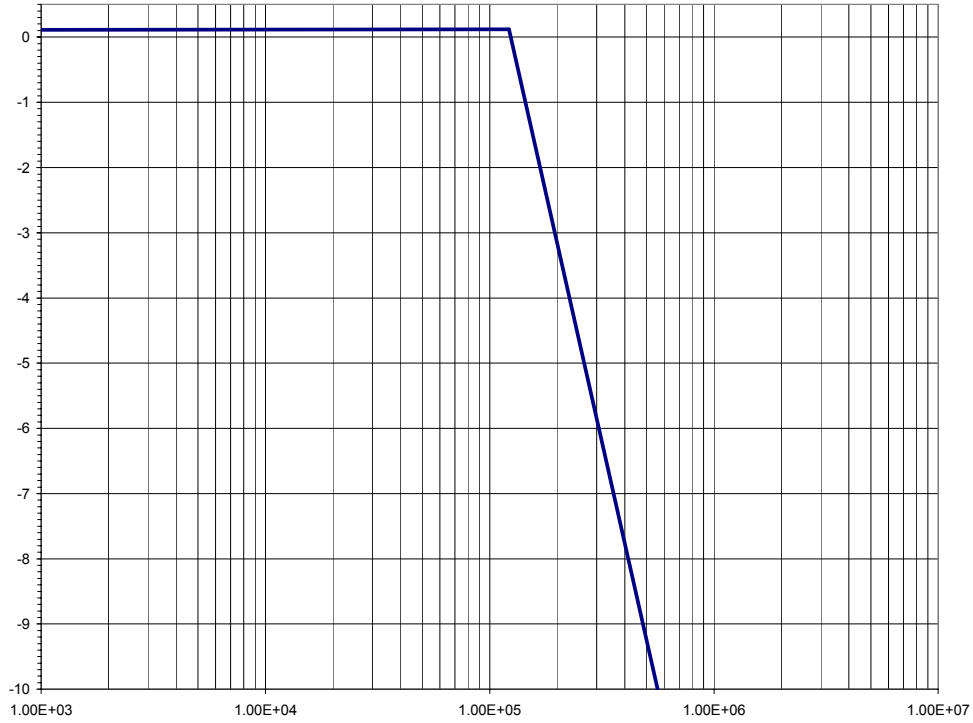


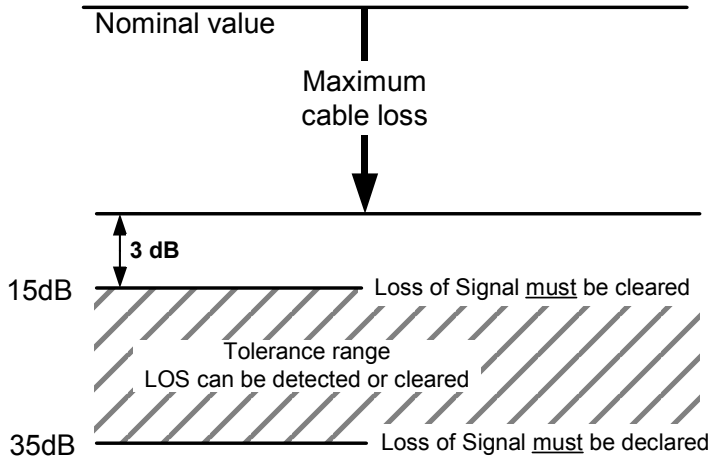
Figure 18: Jitter Transfer

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Receiver Jitter transfer function	below 120 kHz			0.1	dB
Jitter transfer function roll-off			20		dB per decade

ELECTRICAL SPECIFICATIONS (continued)

CMI MODE LOSS OF SIGNAL CONDITION

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
LOS threshold		-35	-18	-15	dB
LOS timing		10	80	255	UI



APPLICATION INFORMATION

EXTERNAL COMPONENTS:

COMPONENT	PIN(S)	VALUE	UNITS	TOLERANCE
Receiver Termination Resistor	RXP RXN	75	Ω	1%
Transmitter Termination Resistor	CMIP CMIN	75	Ω	1%

TRANSFORMER SPECIFICATIONS:

COMPONENT	VALUE	UNITS	TOLERANCE
Turns Ratio for the Receiver		1:1	
Turns Ratio for the Transmitter (center-tapped)		1:1CT	

Suggested Manufacturer: Halo, Tamura, MiniCircuits, Belfuse

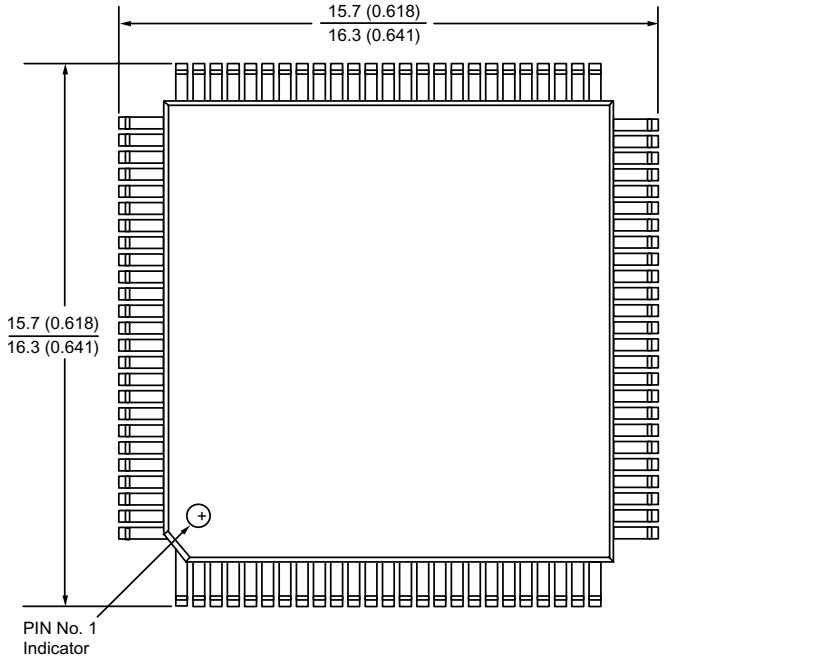
THERMAL INFORMATION:

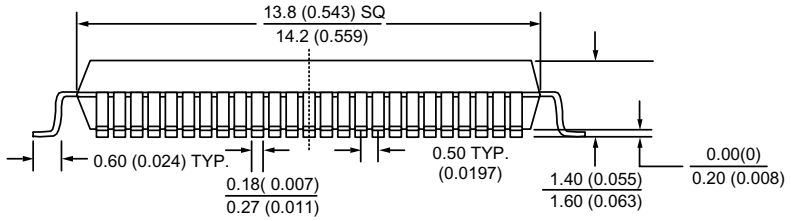
PACKAGE	CONDITIONS	Θ_{JA} (˚C/W)
Standard 100-pin JEDEC LQFP	No forced air; 4-layer JEDEC test board	46

SCHEMATICS

For schematics, recommended transformer part numbers, etc. please check TDK Semiconductor's website or contact your local sales representative for the latest application note(s) and/or demo board manuals.

MECHANICAL SPECIFICATIONS

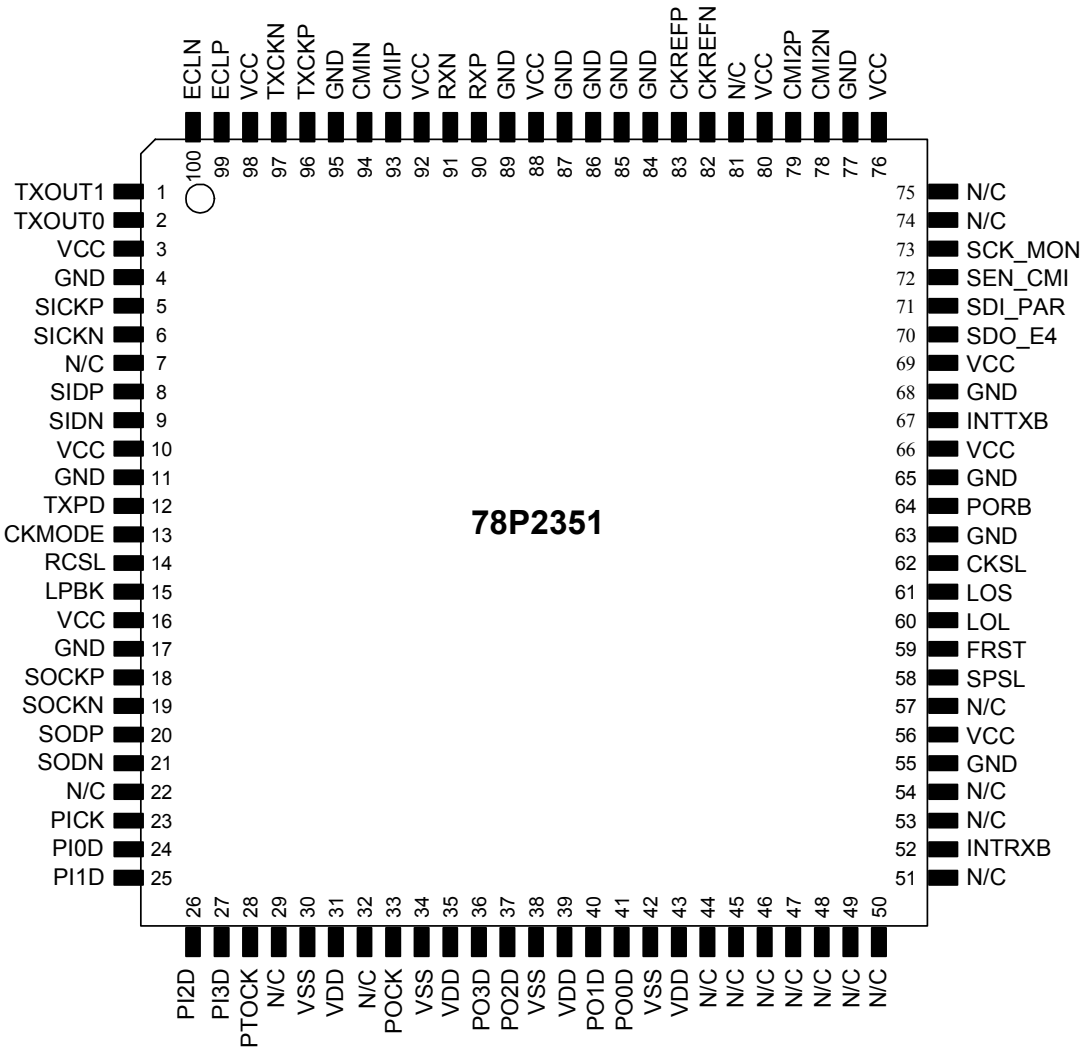




100-pin JEDEC LQFP

PACKAGE INFORMATION

(Top View)



ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
100-pin JEDEC LQFP, *Open-drain type outputs for LOS, LOL, INTTR*	78P2351-IGT /A04	78P2351-IGT xxxxxxxxxC4
100-pin JEDEC LQFP, ***CMOS type outputs for LOS, LOL, INTTR***	**70**P2351-IGT /A04	70P2351-IGT xxxxxxxxxC4
Tape & Reel option	*append* 'R'	n/a
Lead-free option	*append* '/F'	xxxxxxx-xxx xxxxxxxxxC4F

Revison History	
v1-3	**February 13, 2003**: Initial customer release
v1-4	**March 25, 2003**: Modified pinout (pins 67-69) ; Added conditions for LCV ; Added thermal data ; Updated Jitter Specs ;
v1-5	**April 3, 2003**: corrected Pin Description for CMI2P/N
v1-6	**February 11, 2004:** ***Changed to Preliminary Status*** ▪ Added Ordering Numbers ▪ Updated block diagrams and timing diagrams o Notes: New loopback path. Rx data clocked out on falling edge. ▪ Changed default pin type of status pins (LOS, LOL, and Interrupts) to open-drain ▪ Updated DC characteristics and I/O characteristics ▪ Updated Loss of Signal and Loss of Lock descriptions/conditions ▪ Added loop-timing pin control (CKMODE pin) ▪ Added advanced transmit controls (LVPECL Eq., amplitude boosts, and peaking) ▪ Removed CMI LCV detector and Rx Interrupt

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